LLRF4.6 Evaluation Board

Dmitry Teytelman

July 7, 2014

Introduction

This document is an update of LLRF4 documentation packet, describing up-to-date information on 2013 LLRF4.6 revision of the board. The main difference between LLRF4 (last revision 4.2, dated 2009-06-28) and LLRF4.6 is the FPGA. The updated board uses Spartan-6 FPGA in CS324 package. Normally, the boards are assembled with the largest and fastest part fitting the footprint — XC6SLX45-3CSG324. While smaller parts can be used, there is little rationale to do so.

Besides the component changes, several new or improved features have been incorporated:

- Transition from Spartan-3 XC3S1000 to Spartan-6 XC6SLX45;
- New FPGA core supply switcher capable of 2.5 A;
- Power supply jumpers replaced by zero ohm resistors;
- Maximally flat PCB backside for thermal pad mounting on cold plate;
- Reduced parasitics on RF/IF inputs
- High quality stripline LO distribution network, capable of 3 GHz;
- LO 1:8 splitter works to 3.4 GHz;
- LVDS signals routed as 100 Ω differential lines;
- LVDS termination resistors deleted;
- DS1822 thermometer in TO-92 replaced by DS18B20 in SO-8;
- Improved input channel shielding assembly.

The rest of this paper walks through these changes in detail.

FPGA

LLRF4.6 transitions to a more modern Xilinx FPGA. The part is also slightly faster than the old Spartan-3. A short summary of differences between the two parts is shown below. Of course, logic cells comparison is imprecise, since Spartan-6 uses new 6-input LUT architecture. Xilinx uses some fudge factors to convert slice counts to vague "logic cells".

	XC3S1000	XC6SLX45	Notes
Logic cells	17280	43661	
Multipliers	24	58	DSP48A1 in S6
BlockRAM	24	116	18kbits

One quirk of LLRF4.6 FPGA setup is that two data bits on high-speed DAC interface are driven by dual function pins R15 (`IO_L1P_CCLK_2`) and V10 (`IO_L30N_GCLK0_USERCCLK_2`). The bitfile must be generated with startup clock set to CCLK (`-g StartUpClk:CClk` option of bitgen) for these pins to function as user outputs.

RF/LO Subsystem

At the RF input, parallel LC matching network was removed (never used on the original LLRF4, layout considerations).

LO 1:8 power splitter (4 input mixers, 2 output mixers, power monitor, monitor connector) is now built from 7 Mini-Circuits QCN-series quadrature splitters. These parts cover the range from 220 MHz to 3.4 GHz in multiple bands.

The following parts can be used to populate the board according to the desired LO and RF frequencies:

U13, U21, U22, U23, U24, U25, U26: 2-way LO splitter

220-470 MHz	QCN-3+
330-580 MHz	QCN-5+
425-675 MHz	QCN-7+
450-750 MHz	QCN-8+
800-1375 MHz	QCN-12+
675-1300 MHz	QCN-13D+
1100-1925 MHz	QCN-19+
1350-2450 MHz	QCN-25+
1700-2700 MHz	QCN-27+
2500-3400 MHz	QCN-34+

M1, M2, M101, M102, M103, M104: level 13 mixer

40-2500 MHz	SYM-25DMHW
5-3000 MHz	SYM-30DMHW

RF down- and up-conversion can also be bypassed during production.

IF filters

Many different IF filter designs have been developed for the original LLRF4. Most of these should work well with LLRF4.6. Some have already been updated and tested on the revised board — see the table below. CF is center frequency, BW is the bandwdith, level refers to the bandwidth measurement level (drop in dB from the peak). For narrow filters, 3 dB measurement is appropriate, for wider ones, 1 and 0.5 dB bandwidth is specified. In all cases, full bandwidth from lower to upper magnitude drop points is listed.

	CF (MHz)	BW (MHz)	Level (dB)	FS (dBm)
Tested on LLRF4.6				
50 MHz (original)	48.5	9	3	11
39 MHz (Dimtel)	39	5.5	3	-4
74 MHz (Dimtel)	74	11	3	-3
81 MHz (Dimtel)	81	12.4	3	-3
Wideband (J-PARC)	34.1	68.1	0.5	6
Tested on LLRF4.2				
110 MHz (FERMI)	110	58	3	-7
186 MHz (APEX)	190	28	0.5	-5

DAC outputs are also filtered on the board, with a simple two element filter. Original configuration is 150 nH series inductor followed by 100 pF parallel capacitor. This setup has low-pass response with roughly 41 MHz 3 dB bandwidth. This two element design can be reconfigured for wider bandwidth, high-pass response, or bypassed altogether.

Power Supplies

FPGA 1.2 V core supply has been reconfigured on LLRF4.6. The new switching regulator is based on the LTC3604 from Linear Technologies. Here is a comparison of the new device with the MAX1820X used on LLRF4.2:

	MAX1820X	LTC3604	Units
Output current	0.6	2.5	A
Switching frequency	1	2 (up to 4)	MHz
External sync	Direct	PLL	
Sync frequency	10–16 (÷13)	0.8–4	MHz

The FPGA user I/O pin labeled "SYNC" in the UCF provides the optional synchronization function. Existing designs that used this feature based on the MAX1820X will need to be adapted to the different characteristics of the new regulator chip.

One major problem with the MAX1820X was that changes in external sync drive created large output voltage transients, locking up the FPGA (high power dissipation, no JTAG/USB response). For those reasons, few designs made use of the synchronization capability. With a synchronization PLL, LTC3604 can seamlessly go from free running to synchronized mode and back to free running. Direct synchronization drive (without divide-by-13 as in the MAX1820X) provides for more a flexible FPGA divide ratio.

Another power supply related change in LLRF4.6 is the deletion of 8 power output jumpers. These made sense early on, but not at serial numbers above 100. Jumpers have been replaced by zero ohm 0603 parts, so the regulators can still be disconnected from the loads, if necessary.

LVDS inter-board communication

Since Spartan-6 supports internal differential termination for LVDS, on-board termination resistors have been deleted. Direction and termination options can be specified in HDL code now.

Unfortunately, Xilinx does not support bi-directional LVDS I/O with runtime termination control. So the bit files have to explicitly define inputs and outputs, enabling termination for the inputs. Since the signals are flipped on the cable, it is feasible to define 4 output channels and 4 input channels, with identical bitfile on both FPGAs.

Connector Summary

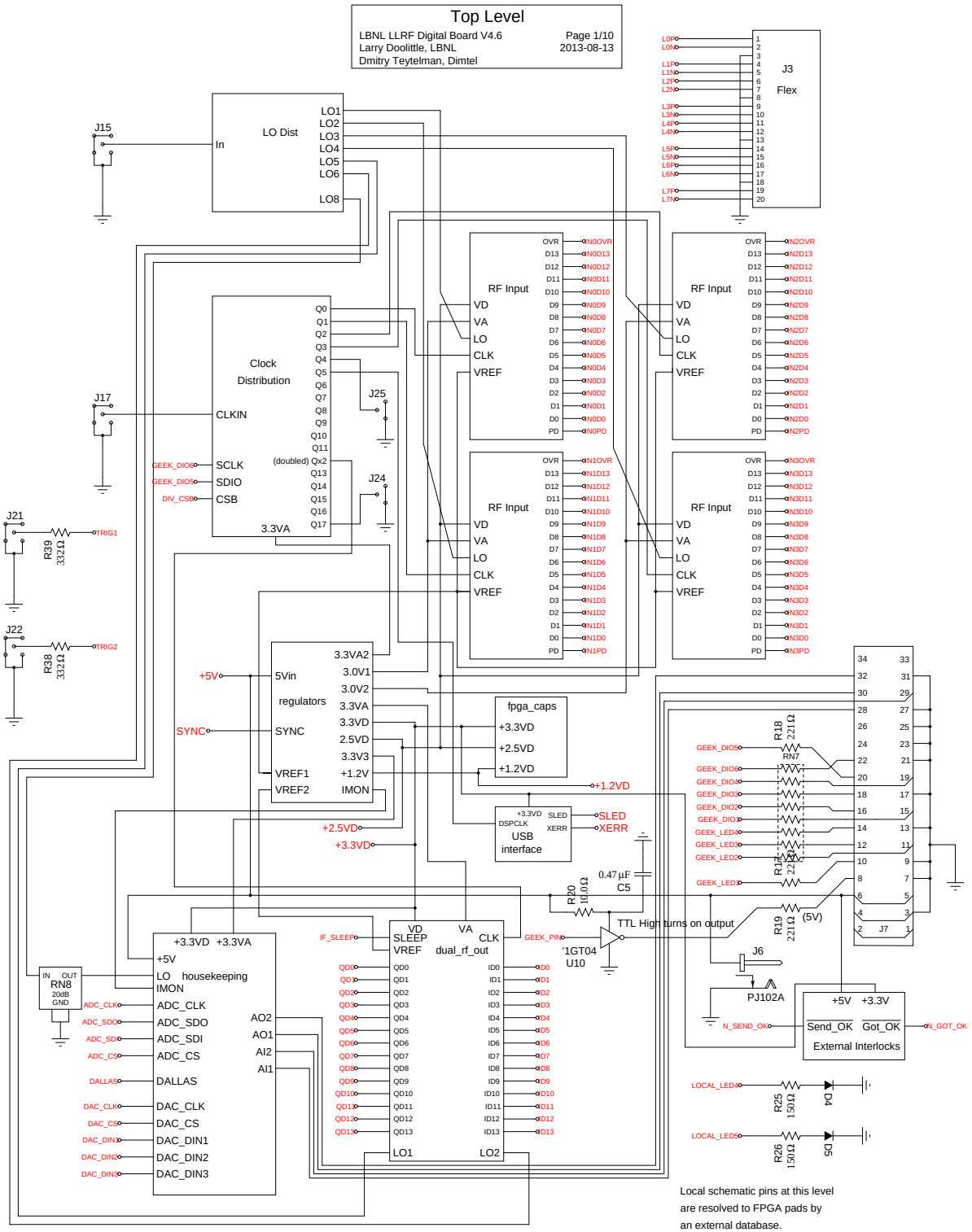
Counterclockwise around the perimeter of the board

J101	SMA	RF/IF input
J201	SMA	RF/IF input
J301	SMA	RF/IF input
J401	SMA	RF/IF input
J15	SMA	LO input (+26 dBm nominal)
J17	SMA	Clock input (+1 dBm nominal)
J7	34-pin header	Geek port (see schematic)
J18	SMA	RF/IF output
J19	SMA	RF/IF output
J20	SMA	Analog output (0 to 2.5V, 2.2 kΩ)
J9	24-pin header	12 channels Analog output (0 to 2.5V)
J8	6-pin Weidmuller	SNS-compatible interlock I/O
J21	LEMO	Trigger
J22	LEMO	Trigger
J6	2.1 mm	+5V, 1.2A pseudo-regulated power input
J1	Type B	USB
J3	20-pin 0.5mm flex	LVDS inter-board communication

Interior test points

J23	U.Fl	LO monitor (remove R809 to maintain match)
J24	U.Fl	ICS83940D output 17
J25	U.Fl	ICS83940D output 4
J26	U.Fl	AD9512 output 3
J27	2mm	IF output channel 2
J28	2mm	IF output channel 1

2mm test points are intended for use with a high-impedance single-ended FET scope probe.


Top Level
LBNL LLRF Digital Board V4.6
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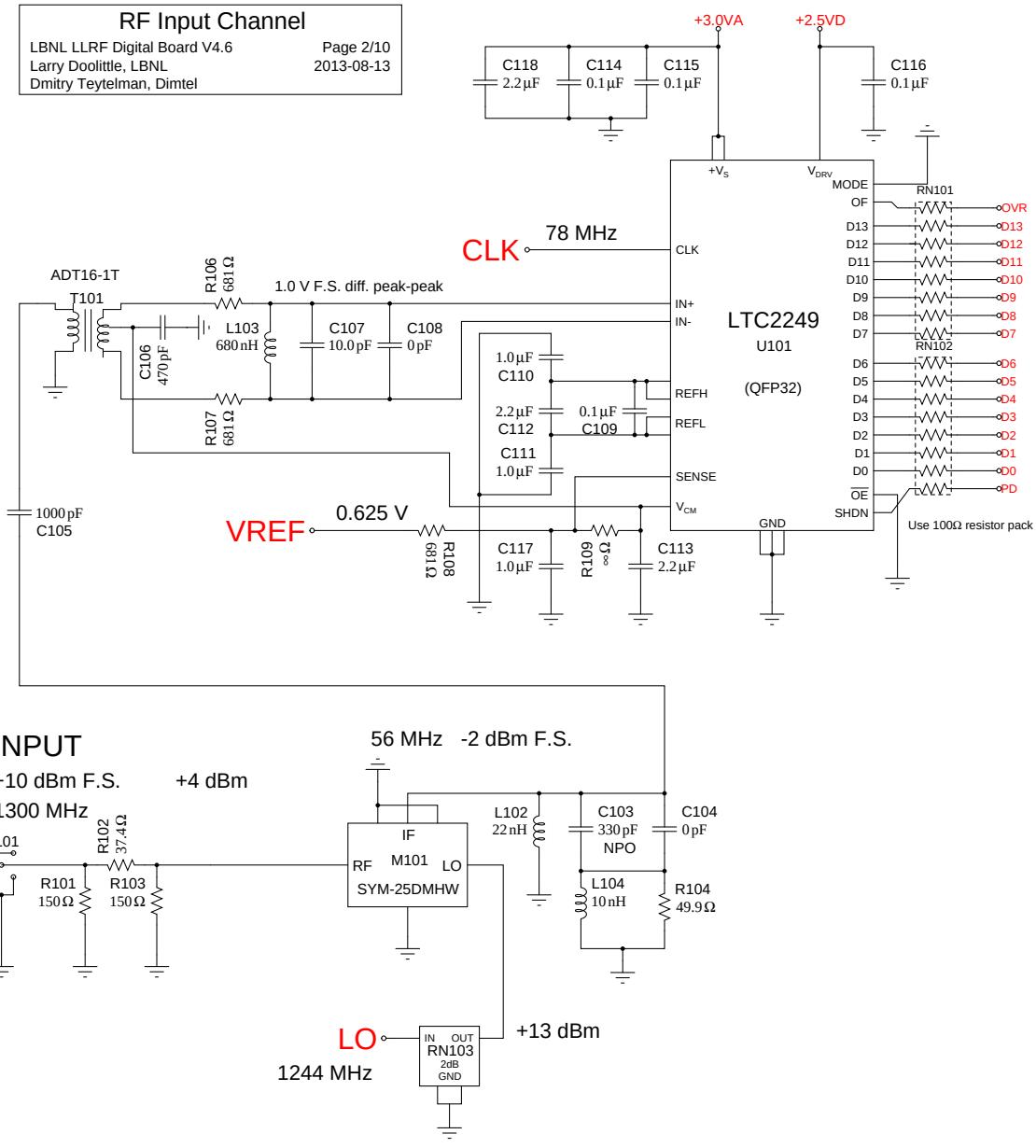
Dmitry Teytelman, Dimtel
Page 1/10
2013-08-13
J3
Flex
J15
In
LO Dist
LO1
LO2
LO3
LO4
LO5
LO6
LO8
J17
CLKIN
Clock
Distribution
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
(doubled) Qx2
Q13
Q14
Q15
Q16
Q17
3.3VA
J25
J24
SCLK
SDIO
CSB
GEEK_DIO6
GEEK_DIO5
DIV_CSB
RF Input
VD
VA
LO
CLK
VREF
OVR
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
PD
N0OVR
N0D13
N0D12
N0D11
N0D10
N0D9
N0D8
N0D7
N0D6
N0D5
N0D4
N0D3
N0D2
N0D1
N0D0
N0PD
N2OVR
N2D13
N2D12
N2D11
N2D10
N2D9
N2D8
N2D7
N2D6
N2D5
N2D4
N2D3
N2D2
N2D1
N2D0
N2PD
N1OVR
N1D13
N1D12
N1D11
N1D10
N1D9
N1D8
N1D7
N1D6
N1D5
N1D4
N1D3
N1D2
N1D1
N1D0
N1PD
N3OVR
N3D13
N3D12
N3D11
N3D10
N3D9
N3D8
N3D7
N3D6
N3D5
N3D4
N3D3
N3D2
N3D1
N3D0
N3PD
J21
J22
R39
332Ω
R38
332Ω
TRIG1
TRIG2
+5V
SYNC
5Vin
regulators
SYNC
VREF1
VREF2
3.3VA2
3.0V1
3.0V2
3.3VA
3.3VD
2.5VD
3.3V3
+1.2V
IMON
fpga_caps
+3.3VD
+2.5VD
+1.2VD
+1.2VD
+2.5VD
+3.3VD
+3.3VD
DSPCLK
SLED
XERR
USB
interface
SLED
XERR
0.47μF
C5
R20
10.0Ω
TTL High turns on output
'1GT04
U10
GEEK_PIN
IF_SLEEP
VD
SLEEP
VREF
VA
CLK
dual_rf_out
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
QD8
QD9
QD10
QD11
QD12
QD13
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
LO1
LO2
+3.3VD +3.3VA
+5V
LO housekeeping
IMON
ADC_CLK
ADC_SDO
ADC_SDI
ADC_CS
DALLAS
DAC_CLK
DAC_CS
DAC_DIN1
DAC_DIN2
DAC_DIN3
AO2
AO1
AI2
AI1
RN8
20dB
IN
OUT
GND
R18
221Ω
RN7
R17
221Ω
RN6
R19
221Ω
(5V)
J7
J6
PJ102A
+5V
+3.3V
Send_OK
Got_OK
External Interlocks
N_SEND_OK
N_GOT_OK
LOCAL_LED4
LOCAL_LED5
R25
150Ω
R26
150Ω
D4
D5
Local schematic pins at this level
are resolved to FPGA pads by
an external database.


RF Input Channel
LBNL LLRF Digital Board V4.6
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Page 2/10
2013-08-13
+3.0VA
+2.5VD
C118 2.2µF
C114 0.1µF
C115 0.1µF
C116 0.1µF
+VS
VDRV
CLK
78 MHz
ADT16-1T
T101
R106 681Ω
1.0 V F.S. diff. peak-peak
L103 680 nH
C107 10.0 pF
C108 0 pF
C106 470 pF
R107 681Ω
IN+
IN-
LTC2249
U101
(QFP32)
1.0µF C110
2.2µF C112
0.1µF C109
C111 1.0µF
REFH
REFL
SENSE
VCM
MODE
OF
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
OE
SHDN
GND
RN101
RN102
OVR
PD
Use 100Ω resistor pack
1000 pF C105
VREF
0.625 V
R108 681Ω
C117 1.0µF
R109 ∞Ω
C113 2.2µF
INPUT
+10 dBm F.S.
1300 MHz
+4 dBm
J101
R102 37.4Ω
R101 150Ω
R103 150Ω
56 MHz -2 dBm F.S.
IF
RF
M101
LO
SYM-25DMHW
L102 22 nH
C103 330 pF NPO
C104 0 pF
L104 10 nH
R104 49.9Ω
LO
1244 MHz
IN OUT
RN103
2dB
GND
+13 dBm

USB Interface

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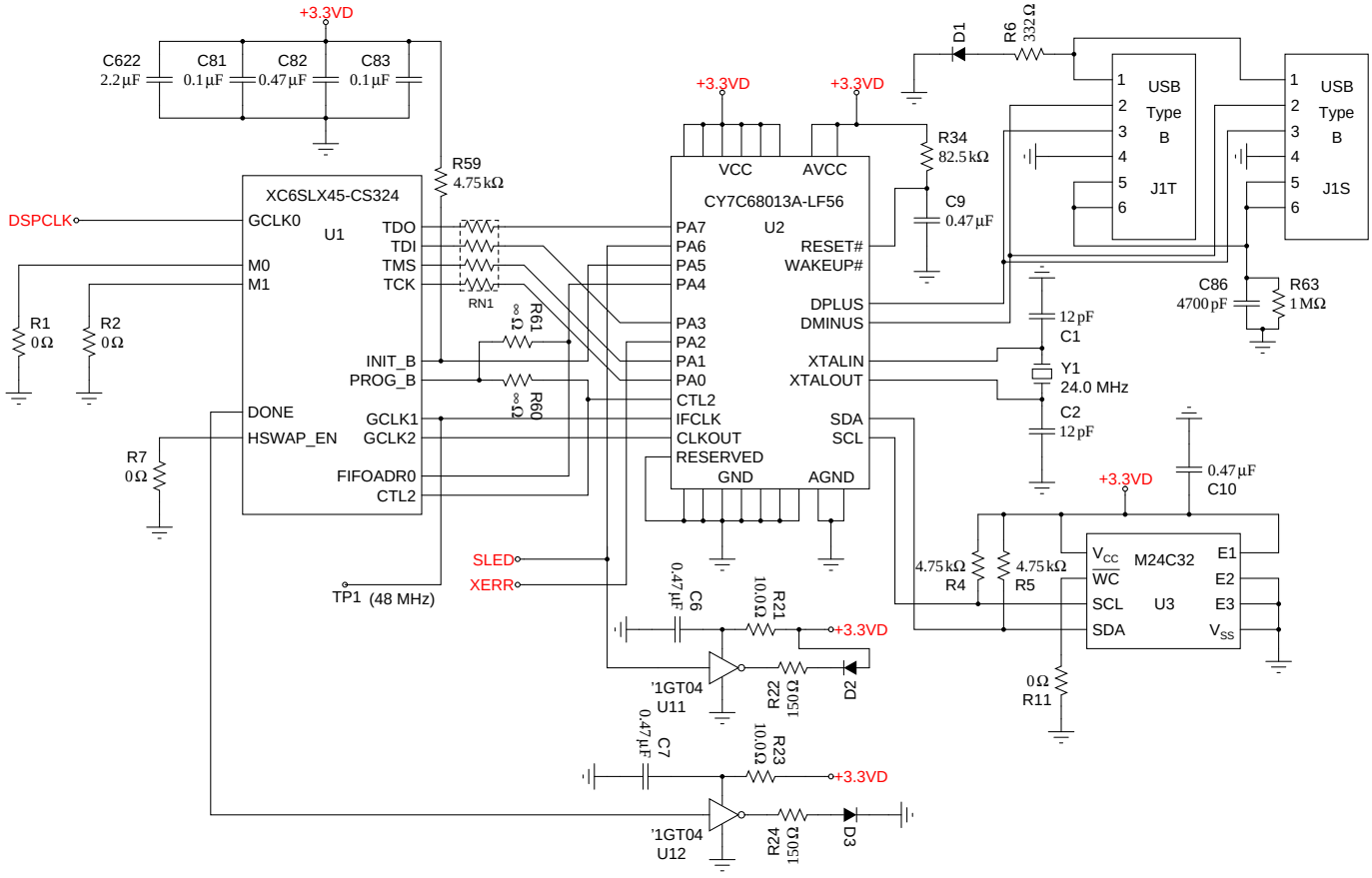

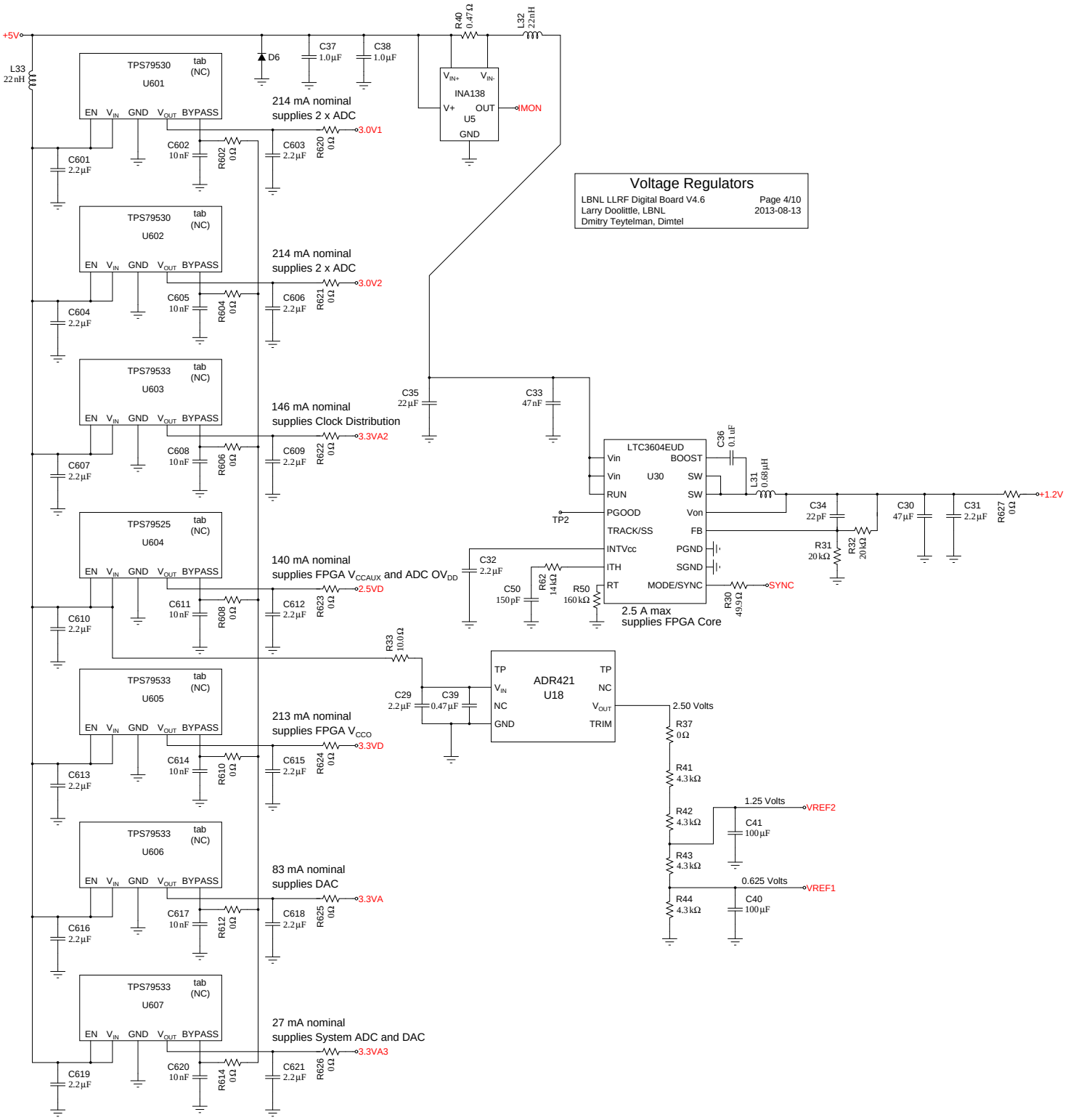

Voltage Regulators

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FPGA Power Capacitors

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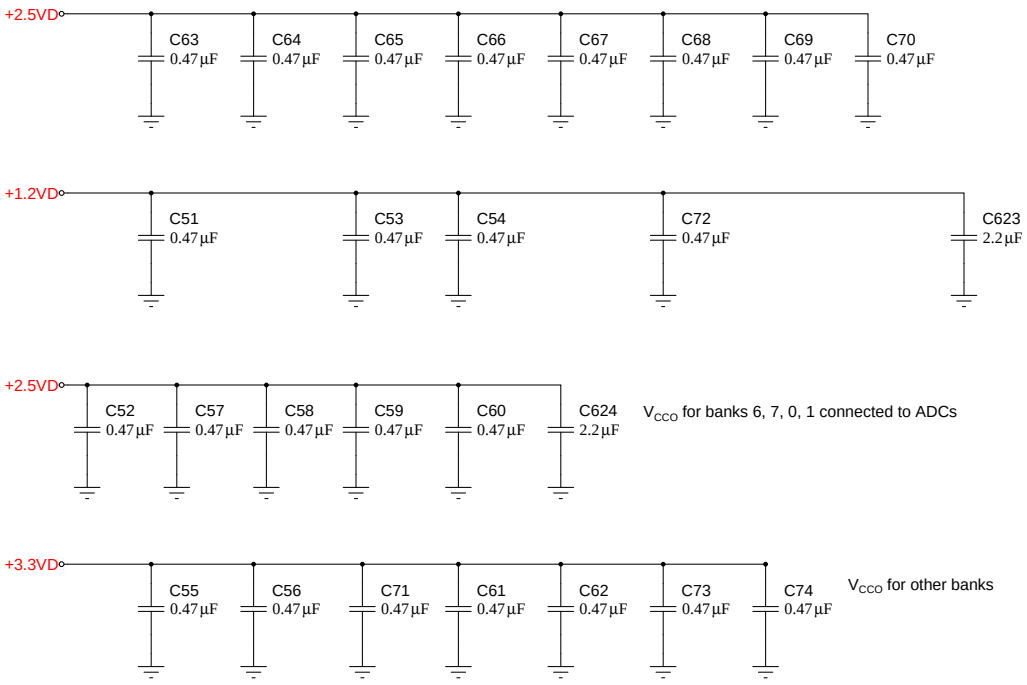

RF Output Channels

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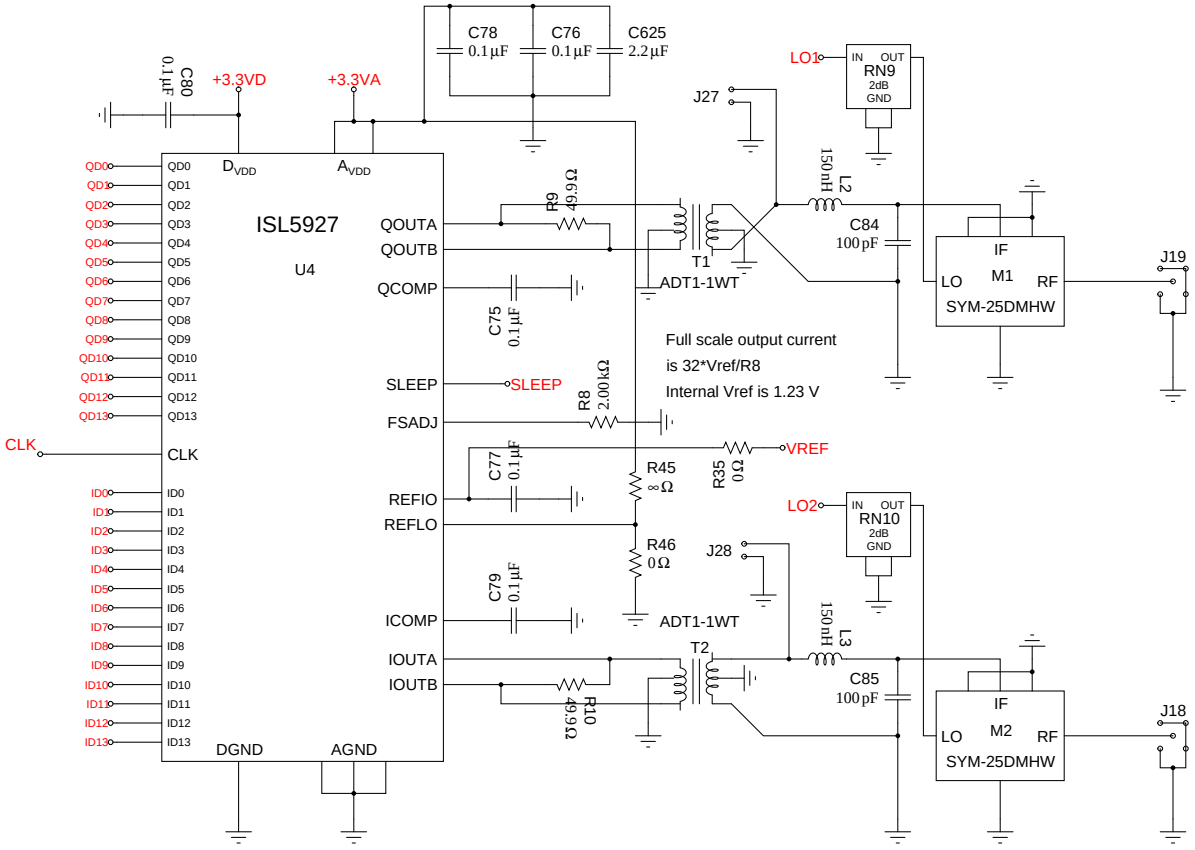

Clock Distribution

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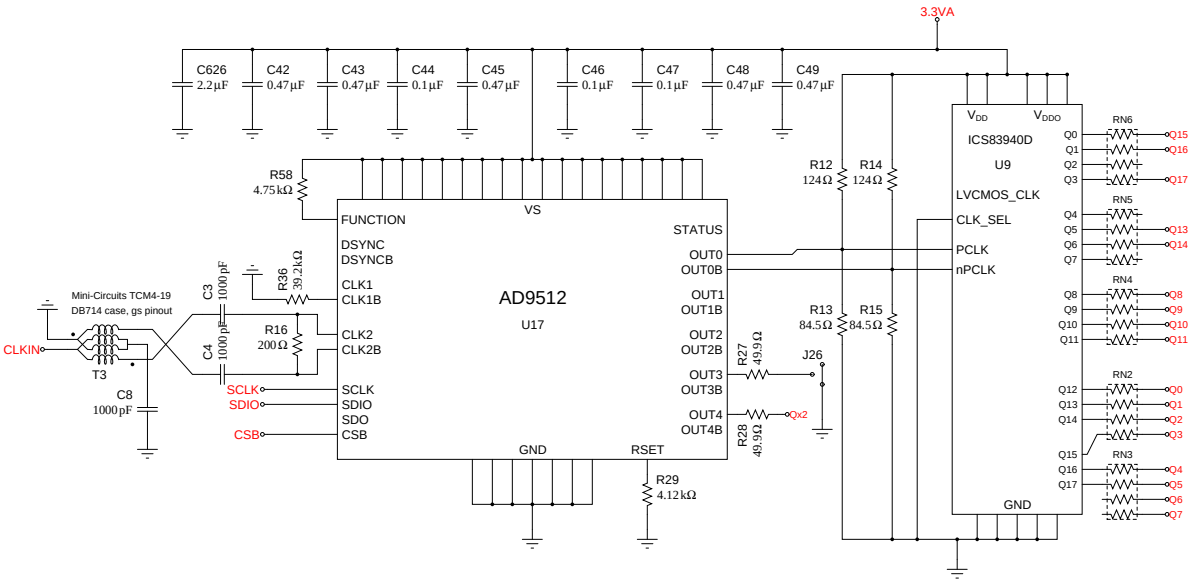

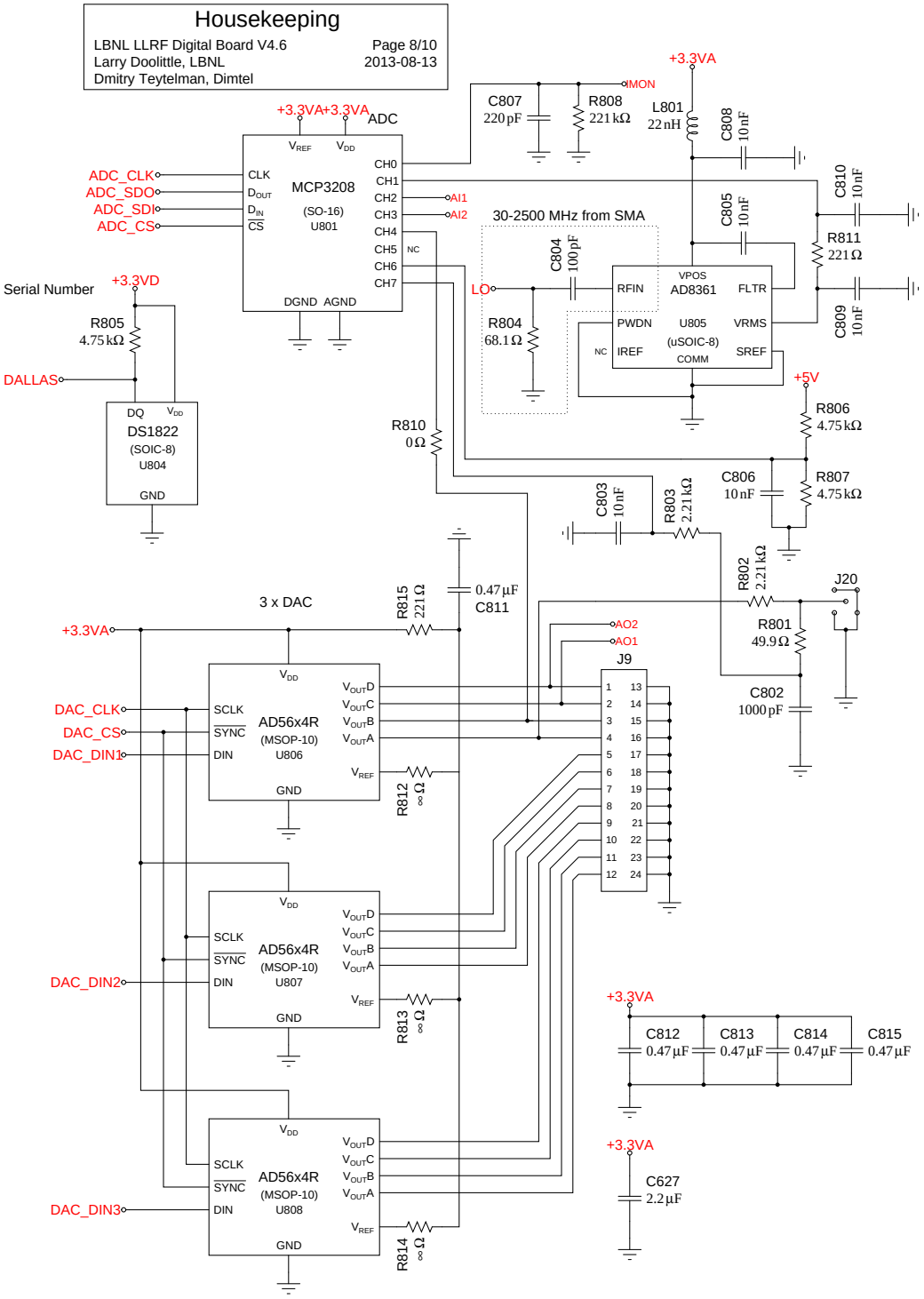
Housekeeping
LBNL LLRF Digital Board V4.6
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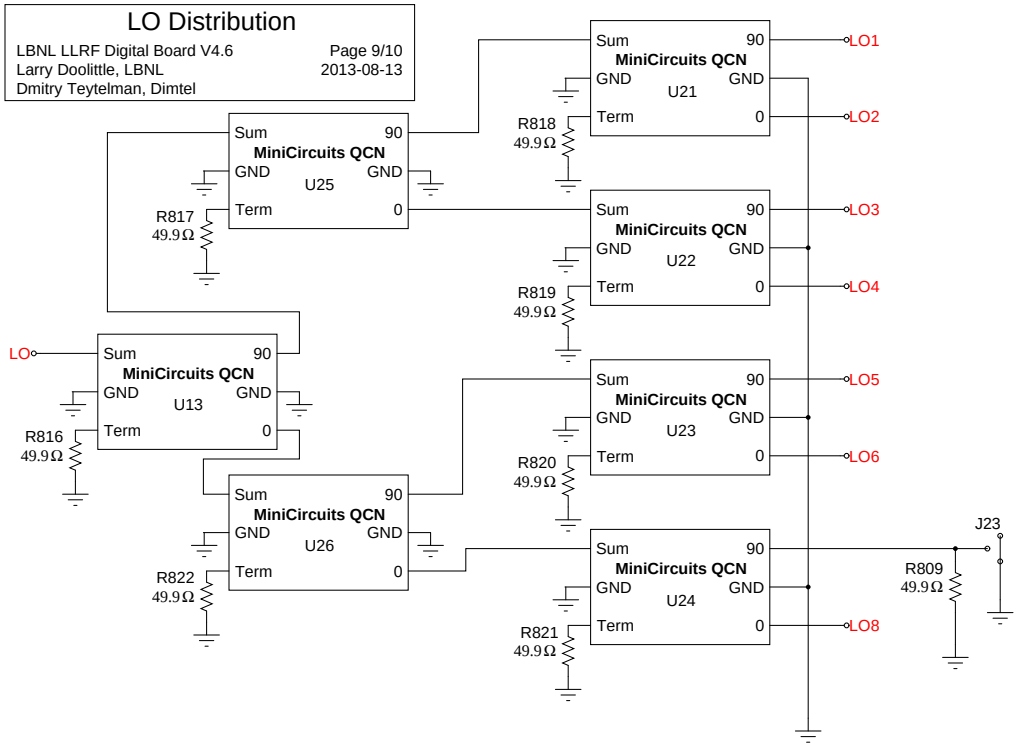
Dmitry Teytelman, Dimtel
Page 8/10
2013-08-13
+3.3VA
IMON
C807 220 pF
R808 221 kΩ
L801 22 nH
C808 10 nF
C810 10 nF
C805 10 nF
R811 221 Ω
C809 10 nF
+3.3VA+3.3VA
ADC
MCP3208
(SO-16)
U801
ADC_CLK
ADC_SDO
ADC_SDI
ADC_CS
CLK
DOUT
DIN
CS
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
NC
AI1
AI2
DGND AGND
30-2500 MHz from SMA
C804 100 pF
LO
RFIN
AD8361
VPOS
FLTR
PWDN
U805
(uSOIC-8)
VRMS
IREF
SREF
COMM
R804 68.1 Ω
Serial Number
+3.3VD
R805 4.75 kΩ
DALLAS
DS1822
(SOIC-8)
U804
DQ
GND
+5V
R806 4.75 kΩ
R810 0 Ω
C806 10 nF
R807 4.75 kΩ
C803 10 nF
R803 2.21 kΩ
R802 2.21 kΩ
J20
3 x DAC
R815 221 Ω
0.47 µF
C811
R801 49.9 Ω
C802 1000 pF
AO2
AO1
J9
+3.3VA
DAC_CLK
DAC_CS
DAC_DIN1
SCLK
SYNC
DIN
AD56x4R
(MSOP-10)
U806
VOUTD
VOUTC
VOUTB
VOUTA
VREF
GND
R812 ∞ Ω
DAC_DIN2
U807
R813 ∞ Ω
DAC_DIN3
U808
R814 ∞ Ω
+3.3VA
C812 0.47 µF
C813 0.47 µF
C814 0.47 µF
C815 0.47 µF
+3.3VA
C627 2.2 µF


LO Distribution
LBNL LLRF Digital Board V4.6
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Page 9/10
2013-08-13
LO
Sum
90
MiniCircuits QCN
GND
GND
Term
0
U13
U21
U22
U23
U24
U25
U26
R816
49.9Ω
R817
49.9Ω
R818
49.9Ω
R819
49.9Ω
R820
49.9Ω
R821
49.9Ω
R822
49.9Ω
R809
49.9Ω
J23
LO1
LO2
LO3
LO4
LO5
LO6
LO8

Interlock Input/Output

LBNL LLRF Digital Board V4.6 — Page 10/10
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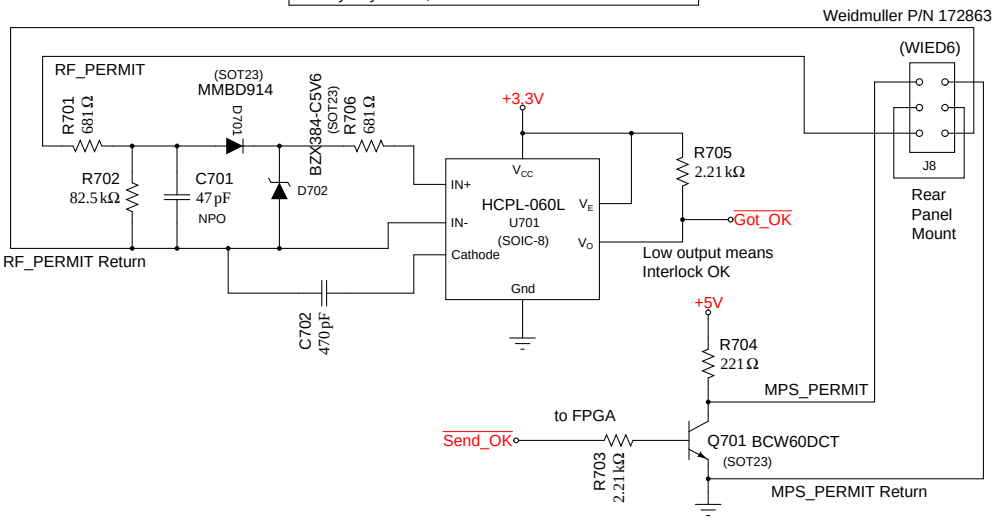
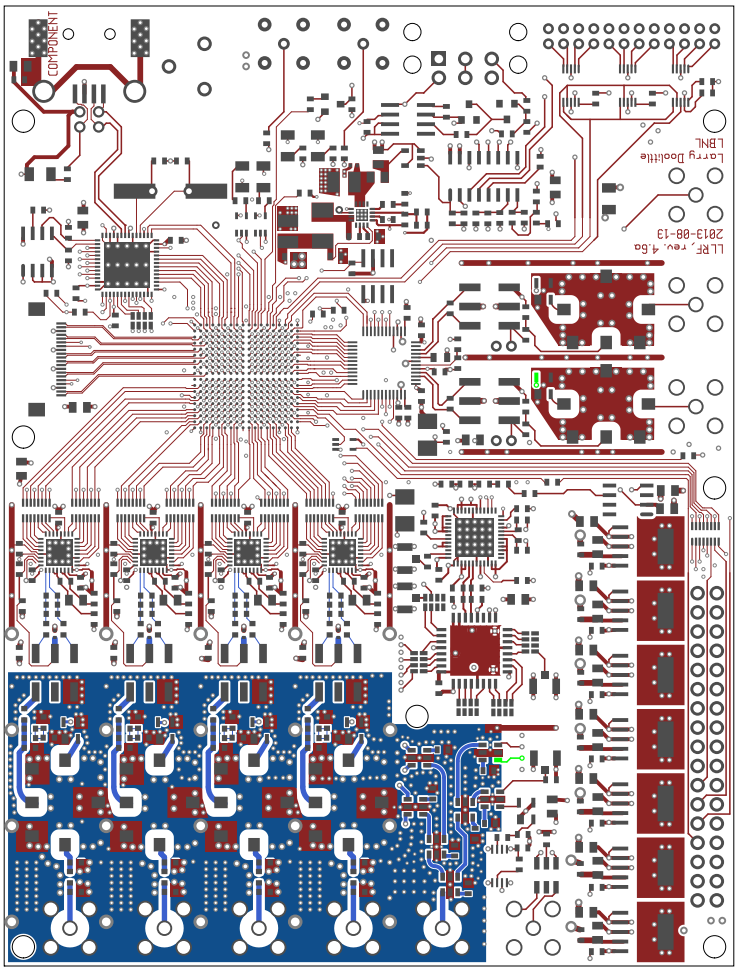
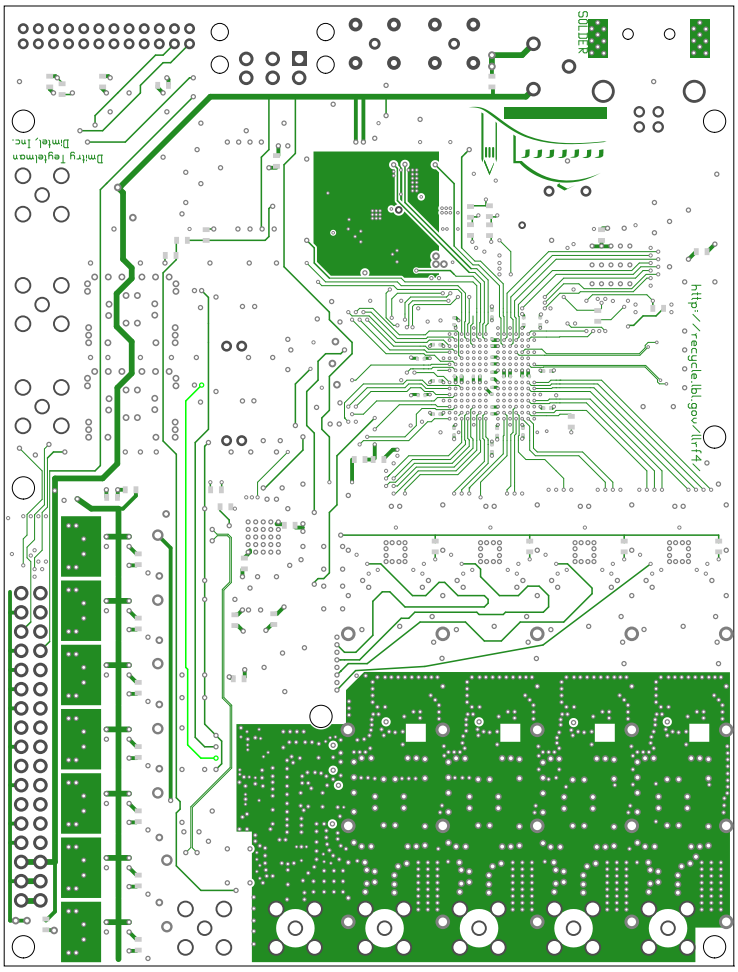
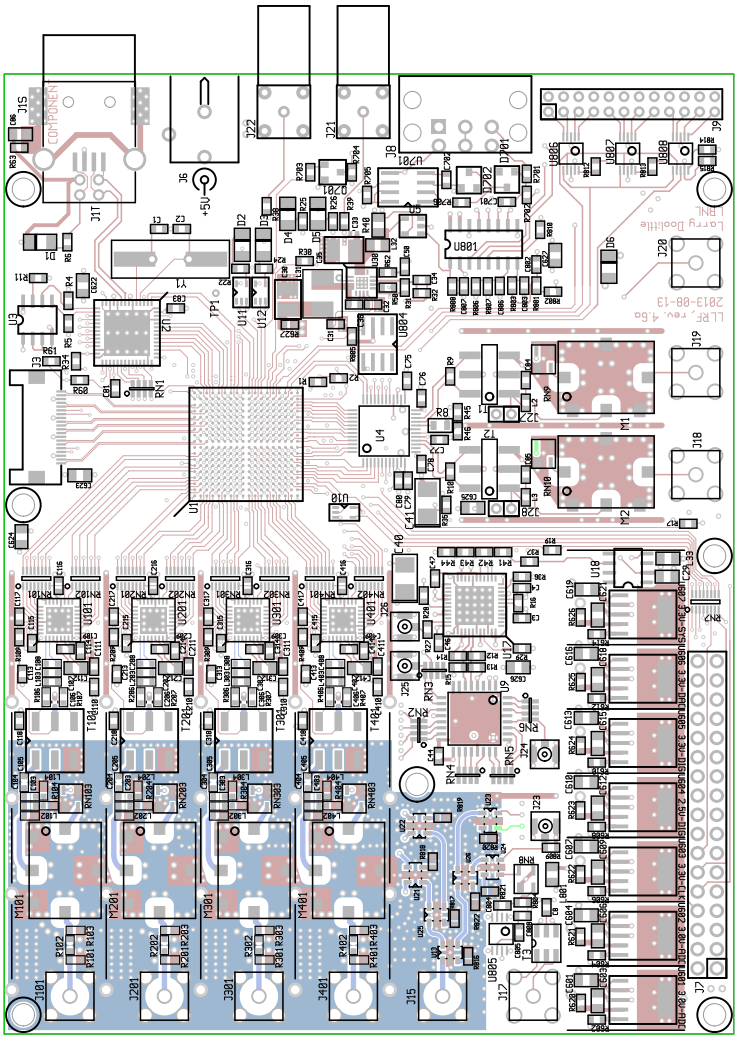




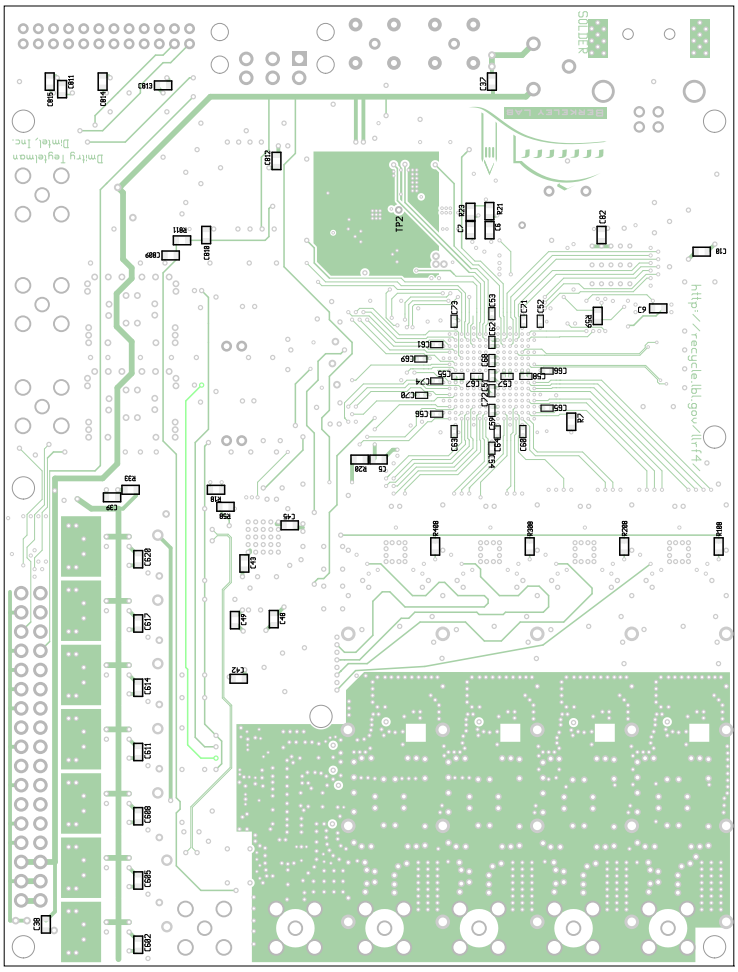
LLRF4, top, scale = 1:1.000
llrf4.pcb



LLRF4, bottom (mirrored), scale = 1:1.000
llrf4.pcb



LLRF4, topassembly, scale = 1:1.000
llrf4.pcb



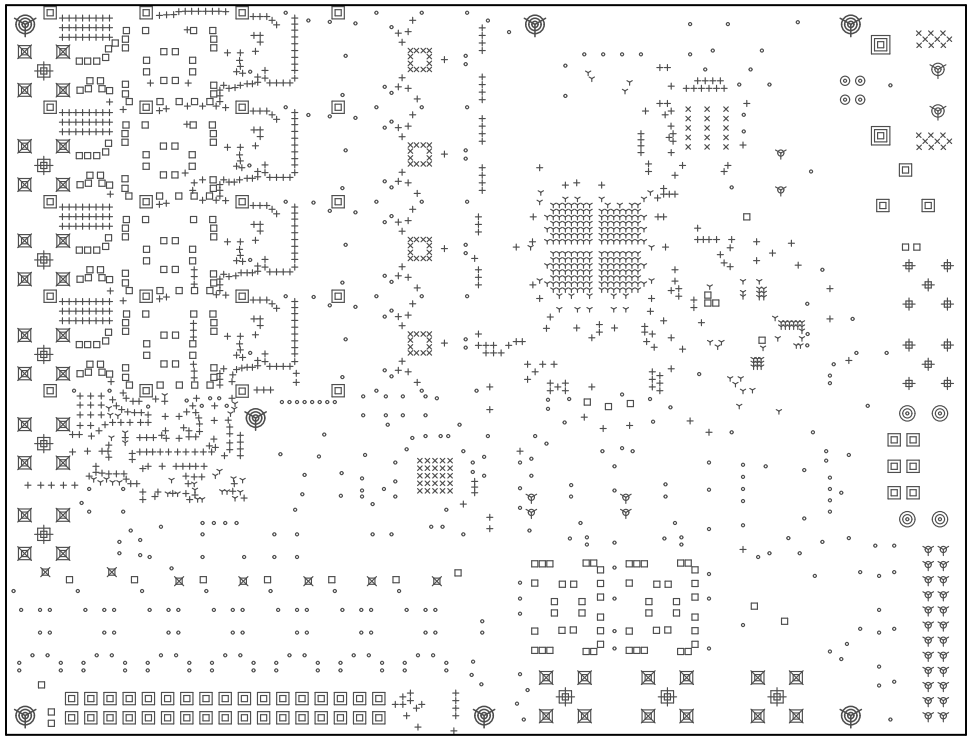
LLRF4, bottomassembly (mirrored), scale = 1:1.000
llrf4.pcb

LLRF4, fab, scale = 1:1.000
llrf4.pcb

There are 16 different drill sizes used in this layout, 1831 holes total

Symbol	Diam. (Inch)	Count	Plated?
˅	0.009	307	YES
+	0.012	657	YES
×	0.014	106	YES
◦	0.015	368	YES
□	0.020	219	YES
⋔	0.030	30	YES
⋕	0.032	10	YES
⊠	0.035	7	YES
⊙	0.036	4	YES
⧈	0.045	63	YES
◎	0.055	2	NO
⋕	0.061	9	YES
⊠	0.067	36	YES
◎	0.090	4	NO
⧈	0.091	2	YES
◎	0.116	7	NO

Title: LLRF4 - Fabrication Drawing
Author: Dmitry Teytelman
Date: Tue 13 Aug 2013 05:45:48 PM GMT UTC
Maximum Dimensions: 5000.000000 mils wide, 3800.000000 mils high



Board outline is the centerline of this 8.000000 mil rectangle - 0,0 to 5000.000000,3800.000000 mils