LLRF9 Low-Level RF Controller

Technical User Manual

Author:
Dmitry Teytelman

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Dimtel, Inc.
2059 Camden Avenue, Suite 136
San Jose, CA 95124
Phone: +1 650 862 8147
Fax: +1 603 218 6669
www.dimtel.com

Contents

1 Regulatory Compliance Information

This equipment requires a ground connection provided by the power source. The exposed metal parts of the unit are connected to the power ground to protect against electrical shock. Always use an outlet with properly connected protective ground.

LLRF9 was designed and tested to operate safely under the following environmental conditions:

- indoor use;
- altitude to 2000 meters;
- temperatures from 15 to 35 °C;
- maximum relative humidity 80% for temperature 31 °C, decreasing linearly to 66% @ 35 °C;
- humidity must be non-condensing;
- pollution category II;
- overvoltage category II;
- mains supply variations of ±10% of nominal.

LLRF9 contains no user serviceable parts inside. Do not operate with the cover removed. Refer to qualified personnel for service.

NOTE: *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

NOTE: *This Class A digital apparatus complies with Canadian ICES-003. Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.*

2 Introduction

LLRF9 is a 9-channel low-level RF (LLRF) controller, designed for lepton storage rings and boosters. LLRF9 is designed to flexibly support different radio frequency (RF) station configurations with one or two high-power source (klystron, inductive output tube (IOT), solid-state amplifier) driving one or two RF cavities. Supported RF configurations are described in more detail in Section 8.

Controller performs vector summing of cavity probe signals, then uses low-latency proportional and integral loops to stabilize the amplitude and phase of the vector sum. Feedback loops are optimized to achieve fast transient response as well as good rejection of perturbations in steady-state operation. Station voltage and phase setpoint can be ramped or modulated using 512 point arbitrary profiles. Profile ramping can be triggered in software or by external opto-isolated trigger inputs. Adjustable time per step allows one to achieve transient profiles from 70 μs to 18.7 s.

LLRF9 includes integrated RF and baseband input interlocks. Nine RF input channels are interlocked against excessive input level. Interlock threshold levels can also be set for eight baseband analog-to-digital converter (ADC) inputs. All internal interlock sources are combined in hardware with an opto-isolated external interlock input. Resulting signal is used to turn off klystron drive and is also available as hardware output for interlock daisy-chaining. All interlock sources are timestamped with $\pm$17.4 ns uncertainty, with automated event sequencing in experimental physics and industrial control system (EPICS).

System supports multiple mechanical tuner motors per cavity, interfacing to motor controllers via RS-485 or Ethernet. Cavity tuning uses phase comparison of probe and forward signals to determine appropriate tuner positions. For cavities with multiple probes and tuners (e.g. five-cell PETRA cavity), LLRF9 provides additional field balancing loops. These loops use differential tuner movement to balance cavity cells for optimal efficiency.

Each of 9 RF input channels is instrumented as follows. Signals are down-converted to baseband and filtered to 4.4 Hz bandwidth. Resulting amplitude and phase values are polled at 10 Hz rate, then converted to appropriate physical units. These values displayed on extensible display manager (EDM) control panels and can be logged or stripcharted using standard EPICS tools.

In addition, LLRF9 includes extensive waveform acquisition diagnostics in time and frequency domains. Time-domain data acquisition captures 16k

samples per input channel on software or hardware trigger. Lengths of pre-trigger and post-trigger portions are freely adjustable. When software trigger is selected, the systems performs 10 acquisition per second. Hardware trigger source is selectable between interlock (for post-mortem diagnostics), external triggers, and setpoint ramp start signal.

Frequency domain diagnostics include an integrated spectrum and network analyzer unit. In the network analyzer mode, a swept sinusoidal excitation signal is added to the station setpoint, and the system's response is detected at the same frequency. An internal multiplexer permits characterization of transfer functions to multiple points within the feedback loop. This tool is critical for feedback loop setup. When excitation amplitude is turned to zero, this module transitions to spectrum analyzer mode, allowing one to observe steady-state spectra.

3 Installation and Maintenance

3.1 Rack Mounting and Ventilation Requirements

LLRF9 is designed to be mounted in a 19″ rack. The unit has three air intakes at the front bottom of the chassis and air exhaust vents at the rear panel. Long term bench-top operation is not advised due to insufficient air intake clearance.

B **WARNING: Do not attempt to mount the unit in the rack using only the front panel screw locations. Use appropriate rails to support the weight of the unit both in the front and the rear.**

At least 1U clearance below the unit is required to ensure proper air supply to air intakes. Do not block the rear panel exhaust vents.

3.2 AC Power Connection

LLRF9 requires a power source of 90 to 264 Vac at 47 to 63 Hz. Maximum input current is 6 A at 115 Vac or 3 A at 230 Vac. Use the AC power cord provided with the unit. Replacement AC power cord must meet the voltage and current requirements listed above.

B **WARNING: This equipment requires a ground connection provided by the power source. The exposed metal parts of the unit are connected to the power ground to protect against electrical shock. Always use an outlet with properly connected protective ground. If it is likely that the protective ground connection has been impaired, the unit must be made inoperative and be secured against any unintended operation.**

3.3 IOC Setup

Setup program is included in the input-output controller (IOC) for configuring the important features of the LLRF9. The program can be executed locally or remotely. For local execution one must first connect a keyboard and a video monitor to the system. For remote setup, use `ssh` after system boot-up to establish connection. In both setup methods the user must login as `root` (initial password is supplied with the system). If the newly received

LLRF9 must be configured remotely (when, for example, a keyboard or a monitor is not available), such configuration can be performed using a dedicated network. Set up a network consisting of the LLRF9, a network hub or a switch, and a remote computer. The LLRF9 is delivered with the following network configuration:

IP address 192.168.1.41
Netmask 255.255.255.0
Gateway 192.168.1.254

Configure the remote computer as follows:

IP address 192.168.1.254
Netmask 255.255.255.0
Gateway 192.168.1.41

Once the dedicated network is configured, remote connection to the LLRF9 can be established by command `ssh root@192.168.1.41`. After logging in locally or remotely, start the setup program as follows:

```
[root@IOC ~]# setup
```

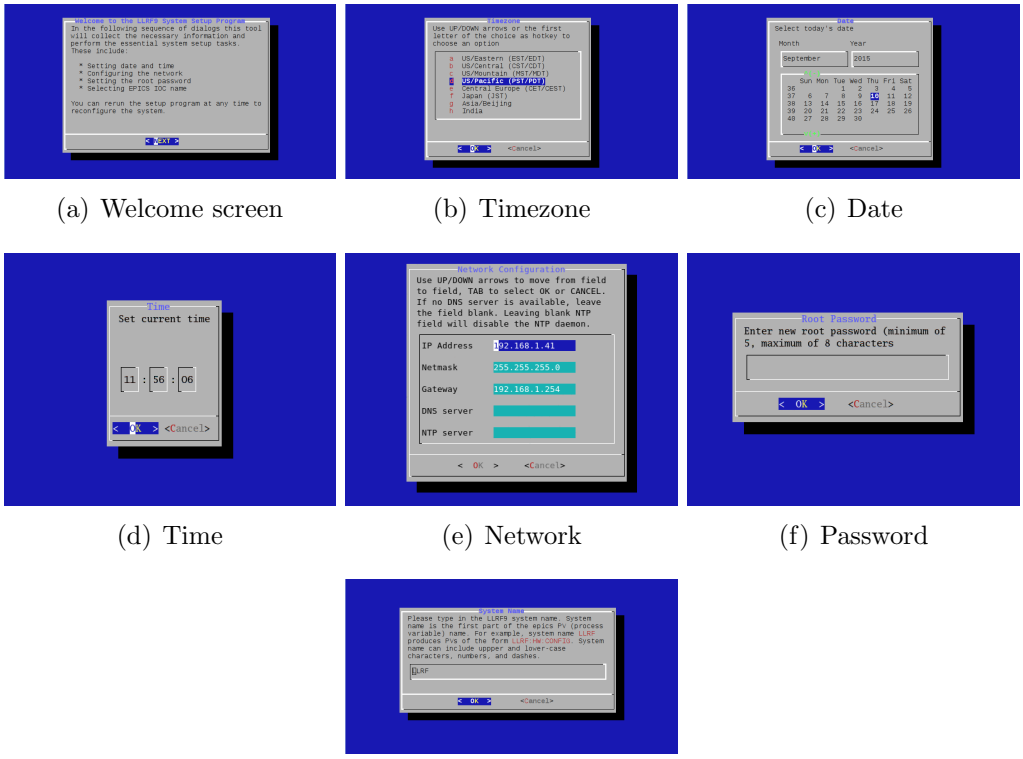
Setup program presents a series of text-mode window dialogs to collect the necessary information for configuring the LLRF9. The following settings are configured in this process: timezone, date, time, network, root password, and EPICS system name.

Setup dialogs are illustrated in Figure 1. Here we provide a step-by-step guide through the setup process.

a) Welcome panel
This panel provides a summary of settings handled by the setup program.

b) Timezone
In this panel, select the appropriate timezone.

c) Date
Set the correct date using the calendar.



(a) Welcome screen (b) Timezone (c) Date

(d) Time (e) Network (f) Password

(g) System name

Figure 1: Setup screens

d) Time

Set the correct time. The initial setting is taken from the current IOC time. If you know the current IOC time to be correct press `OK` quickly to retain the setting as closely as possible.

e) Network

Configure the IOC IP address, network mask and the default gateway as provided by your network administrator. The DNS and NTP server addresses are optional.

NOTE: *Only set the DNS address if the server connection is fast and reliable. Delays in DNS server access can negatively impact the operation of the IOC. Typically DNS address is left blank.*

f) Root password

Type in the new root password. The password must 5 to 8 characters

in length. Please use the standard rules for selecting a strong password (Not based on a dictionary word, a mix of upper and lower-case characters and numbers).

g) Device name

This device name is the second part of the EPICS process variable (PV). All PV names start with `LLRF:`, where `LLRF` is the device name. As delivered the LLRF9 defaults to system name `LLRF` producing PVs of the form `LLRF:HW:CONFIG`. If multiple LLRF units are to be deployed they must be assigned unique device names.

NOTE: *If the setup program is executed remotely and the network address is changed, the* `ssh` *connection will hang at the end of the process. To connect to the IOC, close the existing* `ssh` *session and start the new connection at the newly assigned IOC IP address.*

3.4 Intake Air Filter Maintenance

Three intake air filters are located on bottom front section of LLRF9 and are mounted with 4 6-32 screws each.

B **CAUTION:** *Air filters protect the system from contamination. Operating the unit without the filters or with the filters blocked can lead to overheating as well as to premature failure of the cooling fans.*

B **WARNING: Before performing any work on the filters, power down the system and unplug the AC power cord. Blower blades are exposed when the filters are removed.**

The filters should be periodically serviced to maintain adequate air flow. Vacuuming, washing or replacement are the acceptable maintenance options. Replacement filter is manufactured by Qualtek Electronics Corporation, part number 06325-M.

In order to remove the filters, pull the unit out of the rack. Undo the four mounting screws, retaining each filter. If filter servicing involves washing, make sure the filter is completely dry before reinstallation.

NOTE: *Make sure the custom EMI gasket is reinstalled after filter servicing.*

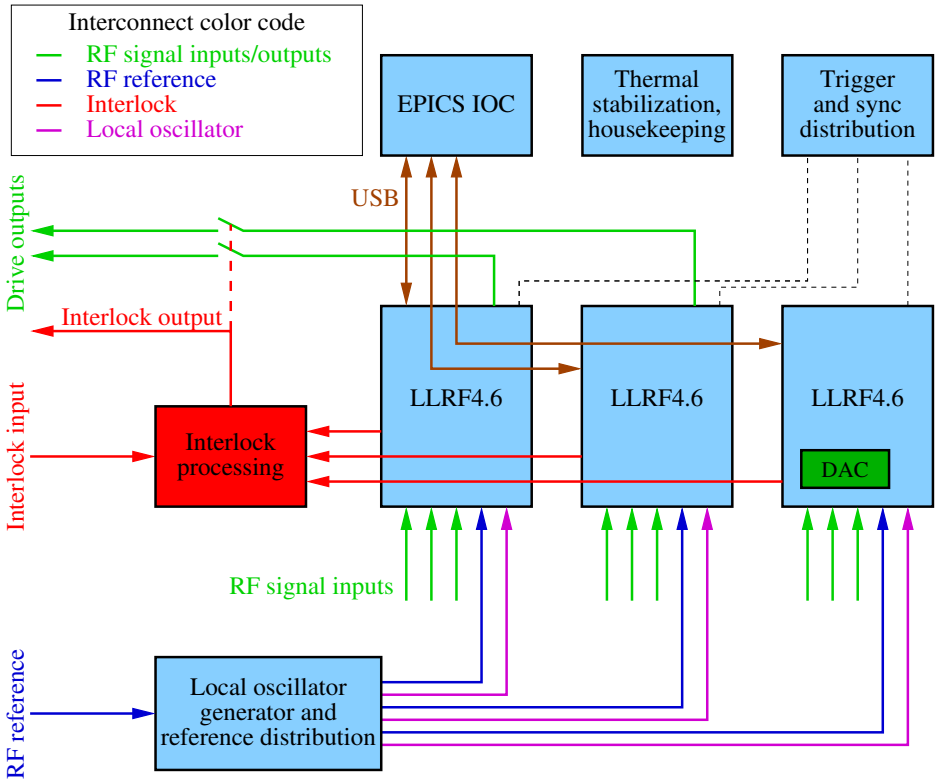


Figure 2: LLRF system block diagram.

4 Hardware

4.1 Overall topology

Overall system topology is illustrated in Figure 2.

Three LLRF4.6 boards are complemented by several additional modules. One of these is an off-the-shelf Linux SBC in the mini-ITX form factor. Another is the LO and interface module with the following functionality:

- Local oscillator (LO) frequency synthesis, amplification, and distribution;
- RF reference distribution;
- Two channels of RF output amplification, filtering, and interlocking;

- Interlock logic;
- Data acquisition synchronization;
- Other housekeeping functions.

LLRF9 chassis is internally partitioned into two compartments: one thermally stabilized for sensitive RF electronics, another for power electronics, IOC, and cooling. In the latter compartment a custom power distribution, interlock, and opto-isolated slow ADC board is installed.

4.2 LLRF4.6

At the heart of LLRF9 system are three LLRF4.6 boards. Each board implements four high-speed ADC and two digital-to-analog converter (DAC) channels. Input channels incorporate downconversion and intermediate frequency (IF) filtering, while the output channels are filtered and upconverted to RF.

A Xilinx Spartan-6 field programmable gate array (FPGA) is used to perform real-time LLRF control, signal acquisition and filtering, interlocks, and many other monitoring and control functions. A detailed description of the board, including design choices, subsystem descriptions, schematics, part information, PCB layout can be found in [1].

4.3 RF input channels

The architecture of LLRF9 dedicates one of four input channels per LLRF4.6 to the RF reference. All phase measurements on the remaining three input channels are then made relative to the reference channel. This approach allows us to reject phase drifts in LO and sampling clock generation systems.

Real-time cavity probe signal processing for closed loop station field control must happen within a single LLRF4.6 module. For a two cavity RF station, board 1 receives two cavity probe signals, performs vector summing and real time feedback processing. The system can also be configured for single cavity operation, in which case one or two RF stations can be independently controlled[1] by one LLRF9 unit. See Section 8 for more detailed description on the supported configurations.

[1] RF stations share the interlock chain, i.e. reflected power event in station A will turn off station B as well.

4.4 RF outputs

LLRF9 has 4 front panel RF outputs. Two of these are designed for power stage drive and are internally amplified, bandpass filtered, and interlocked. Additional two channels are connected directly to the upconversion mixers on LLRF4.6. These can be additionally processed externally and used for monitoring or calibration.

Interruption of the output drive in response to the interlock trip is implemented with dual redundancy. The first control element in this path is the data stream from the FPGA to the output DAC. On interlock trip, FPGA drive to the DAC is set to zero. The second control element is a physical RF switch on LO/interconnect module, providing at least 40 dB isolation in the off state.

4.5 LO signal generation

In order to minimize phase noise contribution from the local oscillator chain, the system uses divide and mix topology, illustrated in Figure 3.

4.5.1 **500** MHz

For the 500 MHz configuration, the IF frequency is chosen as $f_{\mathrm{rf}}/12$. Master oscillator reference signal is divided by 12, low-pass filtered and mixed with the RF, producing signals at $11/12 f_{\mathrm{rf}}$ and $13/12 f_{\mathrm{rf}}$. Using a bandpass filter lower sideband at $11/12 f_{\mathrm{rf}}$ is selected. ADC sampling clock is then derived from the local oscillator as $f_{\mathrm{LO}}/4$. Numerical signal relationships and frequencies are summarized in Table 1.

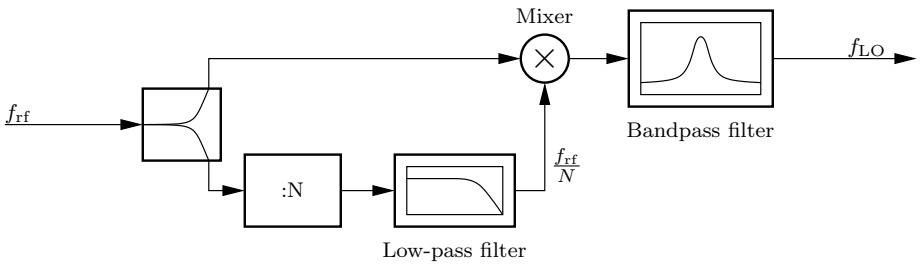


Figure 3: Local oscillator frequency generation

Table 1: Signal numerology and frequencies: 500 MHz

Signal	Symbol	Ratio to f_{rf}	Frequency (MHz)
Reference	f_{rf}	1	499.654
IF	f_{IF}	$\frac{1}{12}$	41.6378
Local oscillator	f_{LO}	$\frac{11}{12}$	458.0162
ADC clock	f_{ADC}	$\frac{11}{48}$	114.5040
DAC clock	f_{DAC}	$\frac{11}{24}$	229.0081

IF is linked to the ADC sampling frequency by the ratio of 4/11. Thus, over four cycles of the IF the ADC will generate 11 samples. These samples, if plotted in polar coordinates of the IF phasor, divide the circle into 11 uniform segments, as illustrated in Fig. 4.

On LLRF4.6 board, DAC outputs are clocked at twice the ADC rate. Synthesizing IF at 229 MHz moves the parasitic line from 72.9 to 187.4 MHz, thus improving its suppression in the output IF and RF filters.

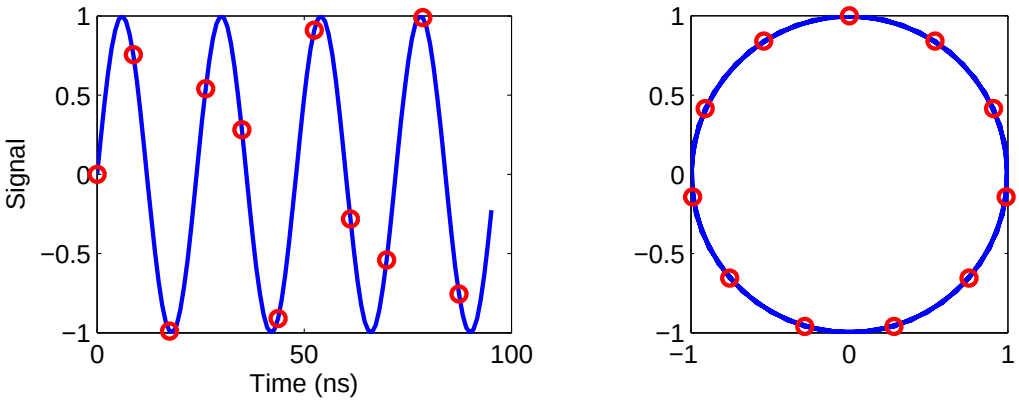


Figure 4: Sampling of the IF signal.

Table 2: Signal numerology and frequencies: 476 MHz

Signal	Symbol	Ratio to f_{rf}	Frequency (MHz)
Reference	f_{rf}	1	476.0000
IF	f_{IF}	$\frac{1}{12}$	39.6667
Local oscillator	f_{LO}	$\frac{11}{12}$	436.3333
ADC clock	f_{ADC}	$\frac{11}{48}$	109.0833
DAC clock	f_{DAC}	$\frac{11}{24}$	218.1667

4.5.2 **476** MHz

In 476 MHz configuration, same divider ratio (12) is chosen, leading to slightly different frequency map, as summarized in Table 2.

4.5.3 **204** MHz

For 204 MHz setup, IF divider ratio is 6. Local oscillator is chosen as the upper sideband of mixing IF and RF, with ADC clock driven by $f_{\mathrm{LO}}/2$. Resulting frequency map is summarized in Table 3.

In this case, IF is linked to the ADC sampling frequency by the ratio of 2/7. Thus, over two cycles of the IF the ADC will generate 7 samples. In this sampling scheme distortion products up to the fifth harmonic of the IF are easily filtered out, with only the sixth harmonic aliasing to the IF.

4.6 Interlock subsystem

Each LLRF9 unit has an external opto-isolated interlock input. System operation is enabled when the input is held high, in order to prevent operation with interlock cable disconnected or damaged. Within LLRF9 the external interlock signal is OR-ed with 17 internally generated interlock bits: 9 for each of the RF input channels and 8 for slow baseband ADC (see section 4.8).

Resulting trip signal is used to turn off the FPGA drive to the DACs and to disconnect absorptive RF switches in the output drive chains. In addition, this signal is available as interlock output on the rear panel. Interlock output

Table 3: Signal numerology and frequencies: 204 MHz

Signal	Symbol	Ratio to f_{rf}	Frequency (MHz)
Reference	f_{rf}	1	204.0000
IF	f_{IF}	$\frac{1}{6}$	34.0000
Local oscillator	f_{LO}	$\frac{7}{6}$	238.0000
ADC clock	f_{ADC}	$\frac{7}{12}$	119.0000
DAC clock	f_{DAC}	$\frac{7}{6}$	238.0000

provides current-limited +5 V when enabled and is pulled low when tripped.

4.7 Digital I/O

LLRF9 has two opto-isolated trigger inputs. Normally these are used to trigger setpoint ramping in booster mode operation. One or both triggers can be used, depending on the system requirements. These inputs can also trigger synchronized waveform acquisition, if needed.

In addition to interlock output with fixed function, LLRF9 provides one digital output driven by an FPGA. This output can be controlled via EPICS or can be tied to some real-time process within the FPGA.

Opto-isolated inputs to LLRF9, including interlock and trigger signal have minimum input high voltage of 3.2 V, but will typically operate down to 2.2 V. The inputs are designed to be driven with 5 or 3.3 V logic signals, capable of sourcing at least 8 mA[2].

4.8 Slow analog inputs

In addition to 9 fast RF input channels, LLRF9 provides 8 slow baseband analog inputs for monitoring external temperatures, voltages, flow rates, etc. These inputs are direct current (DC) coupled and opto-isolated. Slow ADC has four software selectable input voltage ranges: ±10 V, ±5 V, 0–10 V,

[2]Switching thresholds can be customized, if needed.

and 0–5 V. Dynamic input impedance is 21 kΩ in unipolar input modes and 16 kΩ in bipolar ones.

Each of 8 inputs can be configured for current sensing with an internal precision resistor[3], for interfacing with 4–20 mA current loop. Note that analog grounds of all 8 inputs are internally tied together, so when sensing multiple current loop signals one must be careful to avoid ground loops.

Baseband ADC has 12 bit resolution and a maximum sampling rate of 110 ksps. When shared between 8 input channels, per channel sampling rate drops to 13.75 ksps. Each slow ADC channel has an adjustable interlock threshold. Response time ranges from 9 μs for single channel monitoring to 72 μs when all eight are polled sequentially[4].

4.9 Housekeeping

Housekeeping within LLRF9 chassis includes environmental monitoring and control and measurements of internal supply voltages, currents, and critical RF power levels.

Each LLRF4.6 monitors the following onboard sensors:

- Bulk supply voltage;
- FPGA core current;
- Digital temperature sensor (Maxim DS18B20Z+);
- negative temperature coefficient (NTC) thermistor;
- LO power monitor.

In addition, within LLRF9 chassis additional sensors measure:

- 3 NTC thermistors on LO/interconnect board;
- Rotational speeds of 3 chassis blowers;
- Rotational speed of the IOC CPU cooler;

[3] This is a factory configuration option.

[4] Special sampling sequences can be configured, where some inputs are polled more frequently than others. For example, a sequence of channels $0, 1, 2, 0, 1, 3, 0, 1, 4, \ldots$ produces 27 μs latency for channels 0 and 1, and 162 μs for all others.

- IOC CPU temperature;

Aluminum cold plate within LLRF9 chassis is thermally stabilized by three thermoelectric cooler (TEC) modules under closed loop control. A proportional-integral-derivative (PID) loop uses temperature measurements from multiple NTC thermistors to adjust TEC drive currents.

5 Feedback

5.1 Cavity field control

Block diagram of the cavity field control feedback processing path is shown in Fig. 5.

Signals from ADC0 and ADC1 are combined in the vector sum block. If only one cavity is being controlled, vector sum gain for ADC1 is set to zero. Resulting IF frequency signal V_t is subtracted from the station reference signal. The error signal is processed by proportional and integral paths to generate DAC0 drive (to power amplifier). An upsampling interpolator converts the signal to the DAC sampling rate.

As it is clear from the block diagram in Figure 5, generation of the station reference signal is somewhat involved. Consider the signal path starting on the lower right, at the input labeled ADC3. This signal is the RF reference channel and it is downconverted to baseband by a digital downconverter (DDC), then transformed from Cartesian to polar coordinates using a coordinate rotation digital computer (CORDIC) module. This produces a measurement of the reference channel's phase relative to the internal reference phase generator (block on the lower left). Subtracting that measurement from the reference phase and adding setpoint phase ϕ_{set} produces station phase reference that tracks the RF reference channel, canceling some of the common-mode phase noise. CORDIC block that produces station reference IF signal (highlighted in light blue) is driven by the station amplitude setpoint V_{set} and by tracking station phase reference.

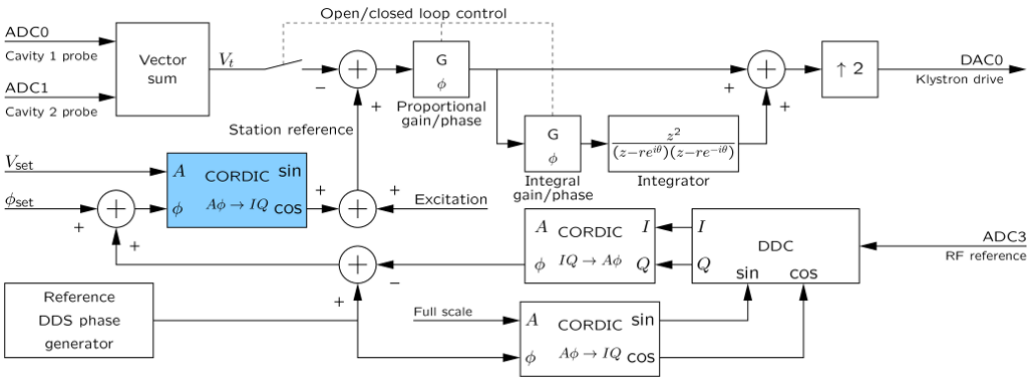


Figure 5: Cavity field control feedback processing.

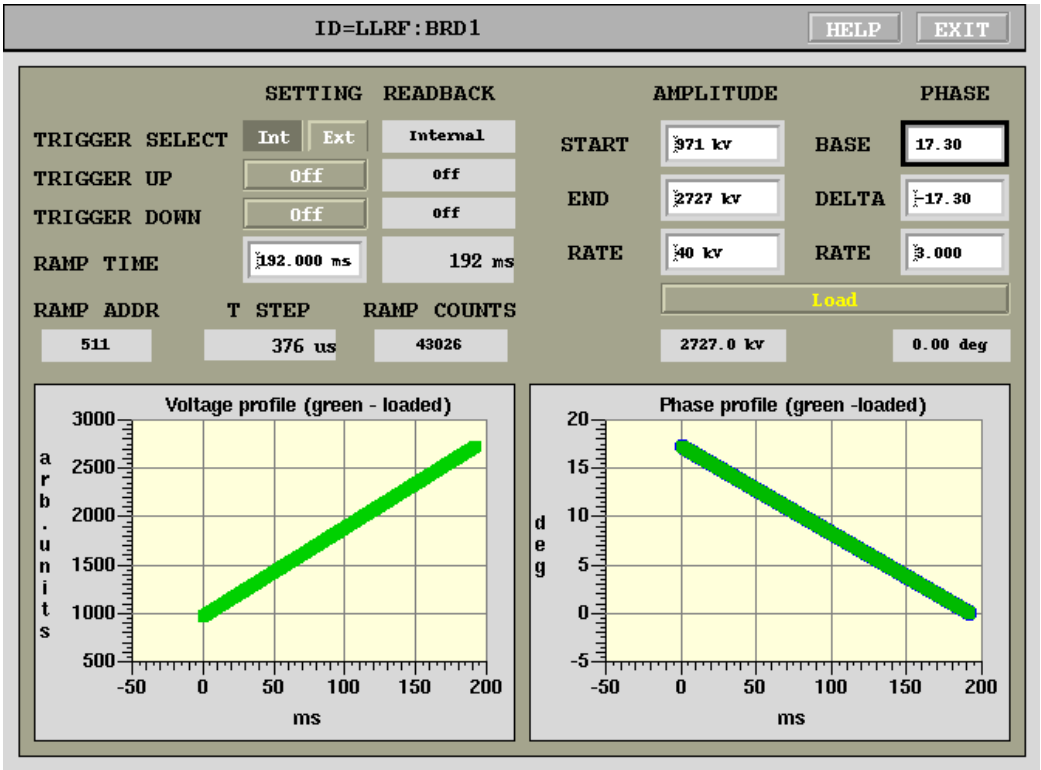


Figure 6: Setpoint control panel.

Excitation signal can be injected into the station setpoint and is used to perform transfer function measurements with the integrated network analyzer. Refer to Section 6.4 for detailed information on the frequency domain diagnostics.

5.2 Setpoint profile

LLRF9 can follow 512 element long amplitude and phase setpoint profiles in order to support transient field ramping. Figure 6 shows the EDM panel for controlling ramping profiles and station setpoint. In standard storage ring operation at constant energy ramping is not used and the station setpoint is controlled by start amplitude value and the base phase angle. Changes in these fields are applied to the actual hardware in a rate-limited way when "Load" control is activated.

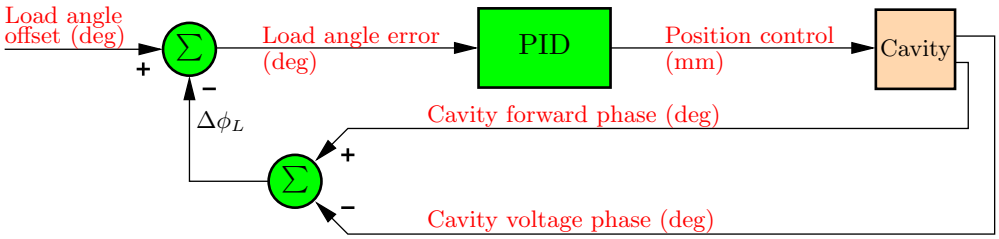


Figure 7: Block diagram of the tuner control loop.

EPICS IOC automatically generates linear amplitude and phase ramps, but can also be configured with arbitrary 512 point profiles. Time extent of the setpoint ramp is adjustable from 36 μs to 18.9 s. Ramping profiles longer than 18.9 s are better implemented by driving LLRF9 setpoints in EPICS from an external process — this allows for tighter synchronization between machine state and RF.

Setpoint ramping can be triggered manually (for testing without beam, for example) or controlled by external hardware triggers.

5.3 Tuner loop

Cavity tuning control is based on the phase comparison of the cavity probe and cavity forward signals. The loop is implemented in EPICS using 10 Hz phase measurement data. Load angle offset setting can be used to guarantee Robinson-stable detuning in low beam loading situations. Tuner loop uses an PID controller, driving steady-state error to zero. A dead-band setting on the load angle error allows the user to trade off the loop performance and the wear of the mechanical components. A simplified block diagram of the tuner loop is shown in Fig. 7.

Output of the tuner loop controller interfaces directly to EPICS motor record [2], which supports many off-the-shelf motion controllers. Motion controller is tasked with driving the actuator — a stepper or a brushless DC motor. The controller also monitors tuner limit switches, making sure the motion stops before mechanical limits are reached.

MDrive® Plus controllers from Schneider Electric [3] include an analog input, which can be used to read out the tuner position potentiometer. To support analog input readback, a modified version of the EPICS driver for these controllers has been created by Dimtel, Inc. and is included with

LLRF9.

LLRF9 supports dual tuners per cavity — a typical arrangement for the popular 5-cell PETRA cavities. In this case, common-mode motion of the tuner motors is used to adjust the resonator frequency, while differential moves allow for balancing the field across different cells. LLRF9 EPICS IOC has a separate field balancing loop which uses two cavity probe signals (center cell and one of the side cells) to maintain the appropriate field profile.

6 Acquisition and Diagnostics

Diagnostic data acquisition and its presentation are critical for successful commissioning, tuning, and operation of the RF system. In LLRF9 each each input RF channel is processed in several ways within the FPGA for diagnostic readout. The system includes two independent time domain data acquisition paths: waveform and scalar. In addition, digital vector network analyzer and spectrum analyzer is built into the each LLRF4.6.

6.1 Scalar acquisition

The scalar path for each input provides amplitude and phase readouts at 10 Hz. These values are computed from the I and Q components generated by the FPGA DDC. Downconverter output is low-pass filtered to minimize aliasing in the 10 Hz sampling process.

Internal synchronization networks in combination with the timestamping logic in the FPGAs guarantee that all 9 measurements are synchronized. That is critical for the situations where cavity probe and forward signals are measured on different LLRF4.6 modules and used for cavity tuner control. In situations where station phase is changing quickly, e.g. during ramping, unsynchronized measurements can lead to large tuner perturbations.

6.2 Channel attributes

6.2.1 Amplitude

Raw I and Q signals are in the units of ADC counts. Each ADC channel includes standard features to convert to the desired physical units, either voltage or power. Calibration constants control conversion from counts to volts or watts and include information about coupling ratios, cable losses, etc. Channel configuration panel (EDM) is shown in Figure 8. The user can select output format as voltage or power, and set the appropriate units. Amplitude calibration is split into two components: channel full-scale power and the coupling ratio. Channel full-scale power setting is linked to the physical hardware, while the coupling ratio combines the measurement path parameters: directional coupler coupling factor, cable loss, units conversion.

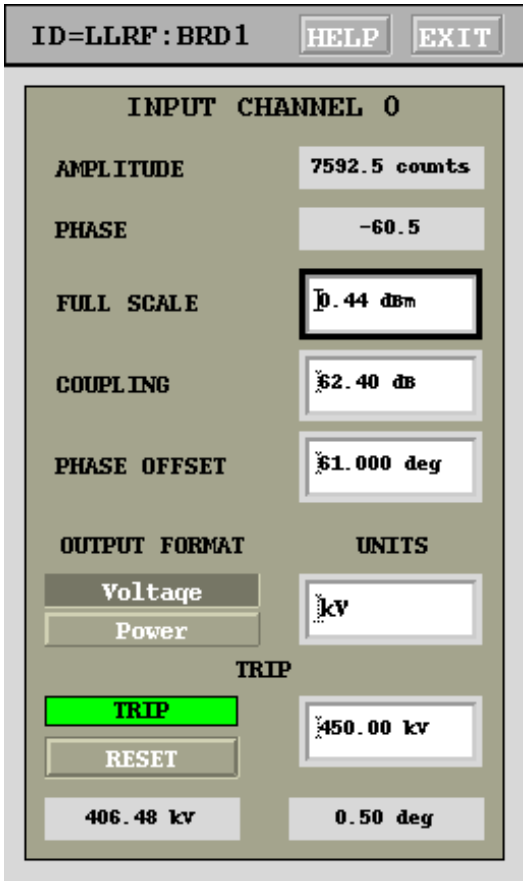


Figure 8: Measurement channel calibration control panel.

6.2.2 Phase

Phase values of the raw DDC output data have no absolute meaning. EPICS driver reads out the four channels, then subtracts the reference channel phase from the three measurement channels.

At this point the phase reflects the difference between the master oscillator reference and the monitored signal at the chassis input. Phase offset field in the calibration panel is used to convert the phase reading to that at the physical location of interest. For example, cavity forward power phase readout should be adjusted to be in phase with the cavity probe at zero loading angle.

Figure 9: Waveform acquisition configuration panel.

6.3 Waveform acquisition

In addition to the scalar readouts, the system also supports waveform acquisition of raw ADC data. Acquisition depth is 16384 samples per input channel. Figure 9 shows the acquisition controls panel. Pre- and post-trigger capture is supported, especially useful for post-mortem data acquisition. When software trigger is selected, waveforms are acquired and read out 10 times a second. Hardware trigger can come from the interlock event, any of the external triggers, or setpoint ramping profile.

In a typical configuration, waveform acquisition engine is set to interlock trigger source, with roughly one quarter of the record captured after the trigger. When RF station trips, this captures activity of all input channels, showing signal behavior just before and after the trip.

During system tuning, waveform acquisition can be used to characterize the feedback loop, capturing step response or steady-state behavior.

6.4 Real-time Network Analyzer

Frequency domain diagnostics in LLRF9 include an integrated spectrum and network analyzer unit. In the network analyzer mode, a swept sinusoidal excitation signal is added to the station setpoint, as shown on Fig. 5, and the system's response is detected at the same frequency. An internal multiplexer permits characterization of transfer functions to multiple points within the feedback loop. This tool is critical for feedback loop setup. When excitation

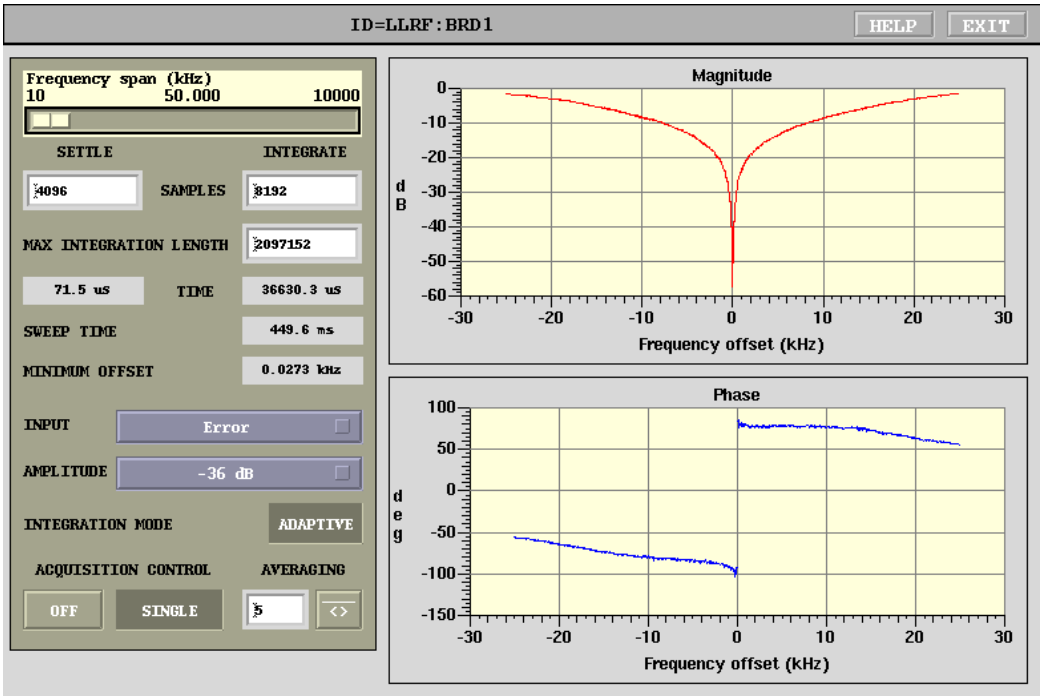


Figure 10: Real-time network analyzer panel.

amplitude is turned to zero, this module transitions to spectrum analyzer mode, allowing one to observe steady-state spectra.

Figure 10 shows the EDM panel for the network/spectrum analyzer. The panel is configured to measure the transfer function from the setpoint to the loop error signal within ±25 kHz of the RF frequency. Minimum offset from the RF in this measurement is 27.3 Hz. Total sweep time is around 450 ms. Both single and continuous measurement modes are supported, as well as sweep-to-sweep averaging. Excitation amplitude is adjustable in 6 dB steps from 0 dB (full scale) to −78 dB. Adaptive measurement mode allows to perform precise small-signal transfer function measurements in presence of a large RF carrier.

7 Interlocks

As described in Section 4, LLRF9 interlock system has 9 RF input and 8 baseband ADC sources. Each interlock channel is timestamped and includes

trip value capture. The IOC performs trip sequence analysis and presents the user with the summary, as shown in Figure 11. First 10 interlock events are ordered according to the timestamps, showing channel names and trip time relative to the first detected interlock event.

7.1 RF input interlocks

Each of 9 monitored RF signals is processed by a peak amplitude detection interlock. The approach is to compare the absolute value of the digitized IF signal to the adjustable threshold. If the value exceeds the threshold, fault signal is asserted. As described in Section 4.5, ADC sampling explores all 11 phase points on the IF waveform over 4 IF periods (96 ns). In the worst case the interlock delay is on the order of that value. Since IF sampling is periodic, depending on the phase alignment of a particular channel, ADC might not sample the peak of the waveform. Mathematical analysis shows that in the worst case sample will be taken at an angle $\pi/11$ away from the

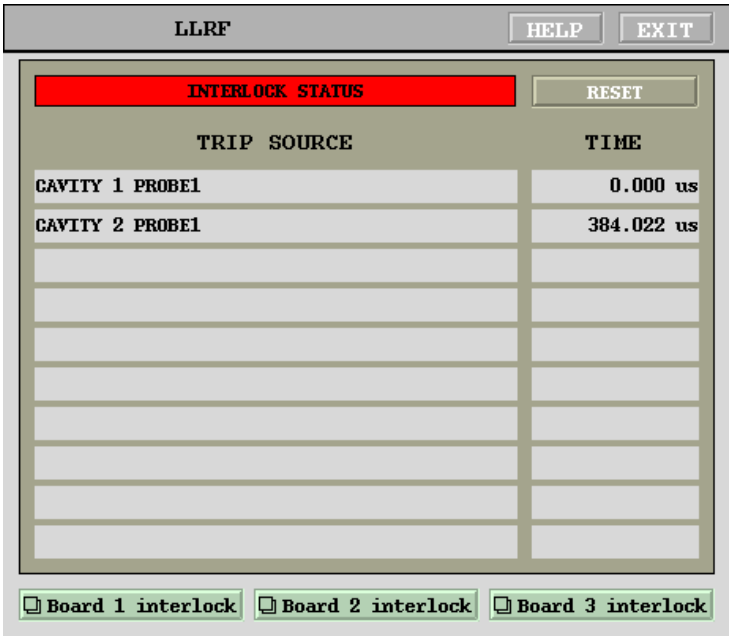


Figure 11: Interlock summary panel.

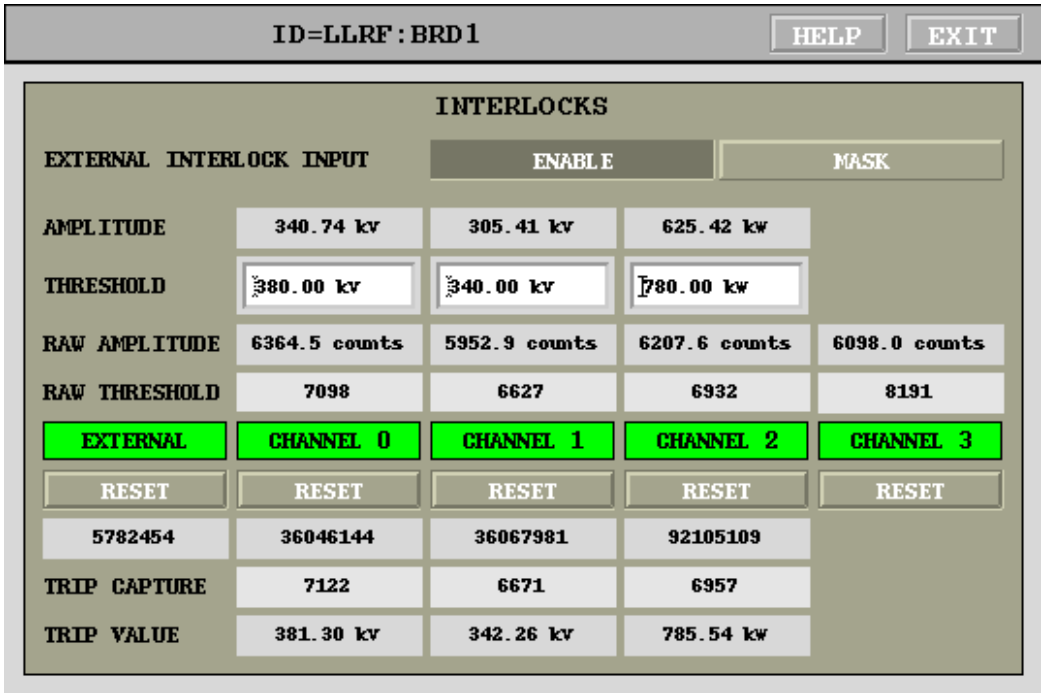


Figure 12: RF interlock detail panel.

peak, resulting in signal amplitude reduction of 0.36 dB (4%)[5].

Figure 12 shows the detailed RF interlock control and information panel for one LLRF4.6.

Each instrumented channel shows readback and threshold values, both calibrated and raw, current trip status, trip event timestamp and captured value.

7.2 Baseband ADC interlocks

Interlock processing for 8 baseband ADC channels takes place in the FPGA and is based on the window comparator model. Each channel has two associated thresholds, low and high. When the input value is outside the range from low to high threshold, interlock is asserted. This structure can be readily adapted to above threshold trip (set low threshold to 0) or below threshold trip (set high threshold to full scale). With the default window comparator

[5]For 204 MHz version, the worst-case error is 0.9 dB or 9.5%

model, inputs such as 4–20 mA can be processed, with the low trip point serving as loop closure detector and the high trip point actually defining the physical parameter threshold.

8 System configurations

LLRF9 supports several different system configurations listed below. Before discussing different options, it is useful to define the terminology. Here, when we refer to an RF stations, we refer to a combination of an single RF power source with one or more cavities and the attendant LLRF hardware.

All station configurations require at least three RF channels per cavity. These channels are cavity probe, forward, and reflected. Cavity probe signal serves as the input to the fast field control loop, as described in Subsection 5.1. Cavity forward signal, together with the probe signal are used by the tuner loop as shown in Subsection 5.3. Finally, the reflected signal is used by fast interlock to prevent damage to the cavity window in case of an arc, beam abort, or other transient events that create poor cavity match.

Theoretically, one could control three individual cavities with one LLRF9. In practice, monitoring of three channels per cavity is the bare minimum, normally additional channels need to be instrumented. Plus, within LLRF9 only LLRF4.6 modules one and two are equipped with thermally stabilized output filtering, interlock, and amplification chains. Module three output is available on the front panel of LLRF9 and could be amplified and filtered externally, but the utility of such solution would be relatively low.

In order to support different system configurations, EPICS IOC in LLRF9 is designed with configurable mapping from physical channels (board 1, channel 2) to logical channels (cavity 1 reflected). The mapping is defined in an EPICS database substitution text file. Additionally, customized front panels are provided, with machine-specific correspondence of physical and logical channels.

1. Single RF station with one power source and one cavity. All 9 wideband RF inputs are available for monitoring signals such as cavity probe, forward, and reflected power, klystron forward and reflected, circulator load forward and reflected, and so on.

2. Single RF station with one power source and two cavities. Cavity monitoring consumes 6 RF inputs (probe, forward, and reflected times

two), with three inputs available to monitor additional signals[6].

3. Two RF stations with two power sources and two cavities. In this case, three mandatory cavity inputs (probe, forward, and reflected) are applied to the first and second LLRF4.6 boards. Refer to Subsection 4.1 for the description of the overall topology of LLRF9. Three remaining inputs can be assigned as needed. In this mode of operation, two stations can be operated nearly independently. The only common link between the stations in this mode is the single chain interlock infrastructure of LLRF9.

These configurations are described below in more detail.

8.1 One station, single cavity, single power source

This configuration is a variation of the two station setup, described in Subsection 8.3. In this case, the second feedback path is unused, freeing up three channels for additional RF signal monitoring.

8.2 One station, two cavities, single power source

In this configuration two cavity probe signals are received by inputs 1 and 2 on a single LLRF4.6board with digital vector combining.

8.3 Two stations, two cavities, two power sources

This operational configuration sends individual cavity signals to separate LLRF4.6boards (1 and 2), with independent feedback loops and power stage drives. Note, however, that LLRF9 has a single interlock chain. So a reflected power event, detected by one station, will activate the interlock for both, turning off power stage drive even for the station that did not suffer interlock condition.

[6]Example configuration from ELSA in Bonn: one klystron driving two five cell PETRA cavities. Three spare inputs are used to monitor klystron forward (and compensate klystron phase shift with operating point), and side probes on cavities to enable the tuner balancing loops

9 Specifications

Table 4: General specifications

Parameter	LLRF9/500	LLRF9/476	LLRF9/204
Operating frequency	500 ± 2.5 MHz	476 ± 2.5 MHz	204 ± 1 MHz
RF reference level	10 ± 1 dBm		
External trigger	2 inputs, rising/falling edge		
Slow analog inputs	8 channels, 12 bits, ±5 V, ±10 V, 0–5 V, 0–10 V		
Chassis	2U 19″ rackmount, 16″ deep		

Table 5: RF inputs

Parameter	LLRF9/500	LLRF9/476	LLRF9/204
Number of channels	9		
Center frequency	500 MHz	476 MHz	204 MHz
Bandwidth	6 MHz	6 MHz	5 MHz
Full-scale input level	+2 dBm		
Channel-to-channel isolation	68 dB		
Spurious-free dynamic range	66 dB		
Readout rate	10 sps		

Table 6: RF outputs

Parameter	Definition
Drive outputs	2
Full scale drive	+8 dBm
Spare/calibration outputs	2
Spare output full scale	−13 dBm

Table 7: Cavity field control specifications

Parameter	Definition
Feedback processing	
Vector sum calculation	2 channels
Feedback loops	Direct and integral
Direct loop delay	270 ns
Real-time reference tracking	Yes
Setpoint modulation	
Trigger source	Internal or external
External trigger inputs	2 (up, down)
External trigger level	TTL/LVTTL, opto-isolated
Ramp profile steps	512
Time per step	70 ns – 37 ms

Table 8: Interlocks

Parameter	Definition
External interlock interface	Daisy-chain input and output
External interlock input	TTL/LVTTL, opto-isolated
RF input interlock comparator	Overvoltage
Worst-case RF interlock error	-0.09 dB
Baseband ADC interlock comparator	Window
Interlock timestamp resolution	35 ns

Table 9: Diagnostics

Parameter	Definition
Time domain	
Raw waveform acquisition channels	12
Samples per channel	16384
Acquisition trigger	Hardware/software
Acquisition mode	Adjustable pre/post-trigger
Acquisition rate, internal trigger	10 waveforms/s
Signal source multiplexer	ADC, cavity sum, loop error, drive
Frequency domain	
Network analyzer	Yes
Spectrum analyzer	Yes
Excitation amplitude adjustment	6 dB steps, from 0 to -78 dB
Number of points	1024
Signal source multiplexer	Cavity 1&2, loop error, drive, loop-back

Table 10: Housekeeping

Parameter	Definition
Voltages	LLRF4.6 bulk supply
Currents	FPGA core
Temperatures	3 digital, 6 NTC, 1 IOC CPU
Fan speeds	3 chassis blowers, 1 IOC CPU fan
Thermal stabilization	3 TEC coolers

Table 11: Input Power Requirements

Parameter	Definition
Input voltage	90–264 VAC
Input current	Max 6 A at 115 VAC
Frequency	47–63 Hz
Voltage selection	Automatic, full range input

10 Warranty and Support

10.1 Warranty

Dimtel Inc. warranties this product for a period of 2 years from the date of the first turn-on at customer's location against defective workmanship or materials. This warranty excludes any defects, failures or damage caused by improper use or inadequate maintenance, installation or repair performed by Customer or a third party not authorized by Dimtel, Inc. Warrantied goods will be either repaired or replaced at the discretion of Dimtel, Inc. The above warranties are exclusive and no other warranty, whether written or oral, is expressed or implied.

10.2 Support

Dimtel Inc. will provide technical support for the product free of charge for a period of 2 years. Such support is defined to include:

- FPGA gateware bug fixes and upgrades;
- IOC software bug fixes and upgrades;
- Client software (display panels, external interface) bug fixes and upgrades;
- Phone, e-mail, and remote access (when allowed by the Customer) support of software and hardware integration.

Free of charge technical support specifically excludes:

- Commissioning with beam;
- Control algorithm development and testing;
- RF and beam dynamics characterization;
- Operational support related to dynamic system operation.

11 Appendix A: Connector Pinouts

11.1 Slow ADC

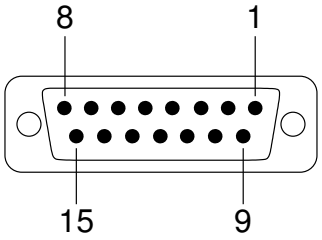


Figure 13: Pin numbering for the DA-15 connector

Eight channel slow ADC inputs are accessible via a 15-pin DA-15 female connector on the rear panel. Pin numbering for this connector is shown in Figure 13. Pin definitions for the 8-channel ADC are provided in Table 12.

ADC signals and common ground reference are galvanically isolated from chassis grounds to prevent ground loops and resulting DC measurement errors. A high quality shielded cable with full 360° connector shielding is recommended.

In software one can select for each ADC input channel one of four ranges: 0–5 V, 0–10 V, ±5 V, ±10 V. Optionally, individual ADC channels can be configured at the factory for current sensing, with internal precision reference resistors.

Table 12: 8-channel ADC pinout

Pin number	Definition
1	Channel 7
2	Channel 6
3	Channel 5
4	Channel 4
5	Channel 3
6	Channel 2
7	Channel 1
8	Channel 0
9–15	Common (isolated)

11.2 Digital I/O

11.2.1 Two pin connectors

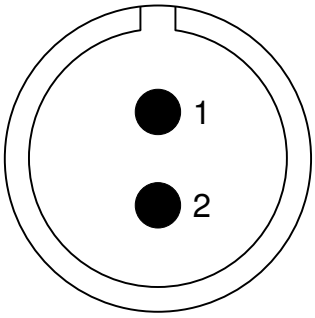


Figure 14: Pin definitions for 2 pin digital input/output (I/O) connectors

Figure 14 shows the pin numbering for the each of five digital I/O connectors. These include interlock input and output, two trigger inputs, and spare output. Connectors used are LEMO® EGG.00.302.CLL and have two isolated signal contacts and a grounded shield.

For two outputs, interlock and spare[7], pin 1 is the active output signal and pin 2 is the ground return. Pin 2 is internally grounded to the chassis. Unloaded output high level is +4.75 V and the output impedance is 220 Ω. When actuated (interlock tripped state), the outputs are pulled down below +0.1 V.

For the three inputs, pin 1 is the positive logic drive input and pin 2 is the ground return. Inputs are individually opto-isolated, i.e. both pins 1 and 2 are galvanically separated from the chassis ground. Input logic levels can be customized during production. Table 13 lists factory-configurable input options for interlock and trigger inputs. Note that the interlock and trigger drivers must be able to provide at least 7 mA of drive current in the high state for the inputs to transition.

Table 13: Digital input options

Logic type	V_{IH} (maximum)	V_{max}
3.3 V LVTTL	2.8 V	3.8 V
5 V TTL	3.9 V	6.0 V
24 V	17.2 V	34.5 V

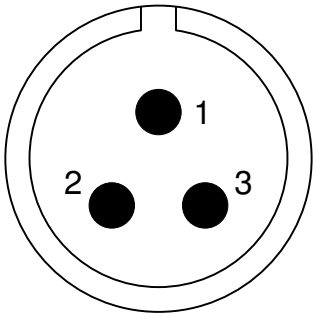


Figure 15: Pin definitions for 3 pin digital I/O connectors

11.2.2 Three pin connectors

In cases when two different threshold levels are specified for digital inputs, it is prudent to differentiate the input voltage standards by using different connectors. For example, with external interlock input at 24 V and trigger inputs at 3.3 V, external interlock can be configured with a 3 pin LEMO® EGG.00.303.CLL connector. Pin numbering for such a connector is shown in Fig. 15. Pin usage is the same as for the two pin connector, with positive logic drive on pin 1 and ground return on pin 2. Pin 3 is not connected.

11.2.3 Four pin connectors

Digital outputs are optionally available in dual output format using a 4 pin LEMO® EGG.00.304.CLL connector. Refer to Figure 16 for the pinout. Pins 1 and 2 maintain the same function as in the two pin connector, with pin 2 internally grounded and pin 1 providing logic level output (below 0.1 V when

[7]By default, spare output is configured as HVPS interlock. HVPS interlock is tripped only in response to slow ADC interlock events and is designed to protect the klystron.

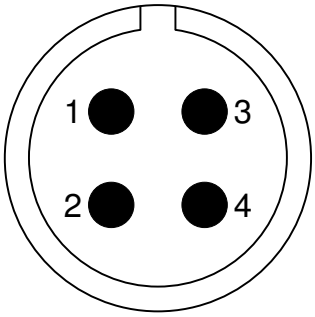


Figure 16: Pin definitions for 4 pin digital I/O connectors

tripped, 4.75 V operational). Pins 3 and 4 are connected to a normally open solid-state relay (0.8 Ω on resistance, 600 mA load current, 60 V blocking voltage). When interlock is enabled, the relay is driven (low resistance state).

11.3 Optional Analog Outputs

LLRF9 can optionally be configured with 1–4 DC coupled analog outputs. These outputs are installed on the rear panel using SubMiniature version B (SMB) connectors. These are driven by the internal 14-bit DACs with 0–2.5 V output range. Short-circuit output current is limited to 30 mA and in normal operation current sourcing or sinking should be kept under 10 mA.

12 Glossary

Glossary

analog-to-digital converter (ADC)

An electronic circuit that converts continuous analog signals to discrete digital numbers. 4, 11–16, 22, 23, 25–27, 34, 35

coordinate rotation digital computer (CORDIC)

A simple and efficient algorithm to calculate trigonometric functions without multiplications. 18

digital-to-analog converter (DAC)

A hardware device to convert a sequence of digital codes to corresponding analog voltages or currents. 11–13, 18, 37

direct current (DC)

In electrical engineering context — a constant signal, either voltage or current. 15, 34

digital downconverter (DDC)

A signal processing structure that translates digital signal from an IF to baseband. 18, 22

extensible display manager (EDM)

A tool that manages a collection of active displays with the ability to create and edit display content as well as the ability to execute the same content resulting in the dynamic presentation of live data. 4, 19, 22, 25

experimental physics and industrial control system (EPICS)

A set of software tools and applications used to develop distributed soft real-time control systems. 4, 7, 9, 15, 19–22, 28, 39

field programmable gate array (FPGA)

A semiconductor device containing programmable logic components and programmable interconnects. 11, 12, 14–16, 22, 27, 30

intermediate frequency (IF)

RF signal processing is often performed at a frequency significantly below the frequency of operation. Signal at an intermediate frequency is typically produced by mixing the high-frequency signal with an offset local oscillator. 11–14, 18, 26, 38, 39

input/output (I/O)

An interface for transferring analog or digital signals to or from the device. 35, 36

input-output controller (IOC)

An embedded computer used to interface the hardware to the control system. 6–9, 19, 21, 25, 28, 30

inductive output tube (IOT)

A high-efficiency vacuum tube used for high-power RF amplification 3

low-level RF (LLRF)

A subsystem responsible for measuring cavity fields and generating drive signals for the high-power RF 3, 11

local oscillator (LO)

An oscillator, offset from the signal frequency by the IF. 10, 11, 16

negative temperature coefficient (NTC)

Negative temperature coefficient associated with a physical property (electrical resistance, thermal conductivity, etc.) means that the value decreases with the increase in temperature. 16, 30

proportional-integral-derivative (PID)

A feedback controller which combines proportional, integral, and derivative responses to achieve disturbance rejection and reference tracking. 16, 20

process variable (PV)

An individual control or readout signal in EPICS 9

radio frequency (RF)

In the accelerator context, a constant frequency constant amplitude signal derived from or phase locked to the storage ring master oscillator. 3, 4, 10, 11, 13–15, 18, 19, 22, 24–30, 39

SubMiniature version B (SMB)

Coaxial RF connector with snap-on coupling 37

thermoelectric cooler (TEC)

A device that utilizes thermoelectric effect (Peltier effect) to create heat flux at a junction of two types of material. 16, 30

References

[1] LLRF4.6 Evaluation Board.

[2] EPICS: Motor Record.

[3] MDrivePlus Family of Integrated Motion Control Products.